A New SiGe Base Lateral PNM Schottky Collector Bipolar Transistor on SOI for Non–Saturating VLSI Logic Design

Abstract– A novel bipolar transistor structure, namely, SiGe base lateral PNM Schottky collector bipolar transistor (SCBT) in Silicon–On–Insulator (SOI) substrate is explored using two–dimensional (2–D) simulation. A comprehensive comparison of the proposed structure with its equivalent PNP HBT is presented. Based on our simulation results, we demonstrate for the first time that the proposed SiGe base lateral PNM transistor exhibits a superior performance in terms of high current gain and cut–off frequency, reduced collector resistance, negligible reverse recovery time and suppressed Kirk effect over its equivalent lateral PNP HBT. Further a simple fabrication process compatible with BiCMOS technology is also discussed.

I. Introduction:

SiGe HBTs are playing a vital role in many applications which require stringent demand on device performance parameters (β, g_m, and f_T) compared to silicon BJT. They satisfy the requirements of RF circuits (LNAs, PAs, mixers, modulators, VCOs, etc), mixed signal circuits (fractional N synthesizers and analog to digital converters) and in the precision analog circuits (Op Amps, band gap references, temperature bias control and current mirrors) by offering high speed (f_T, f_{max}), high current gain, better linearity and most importantly with minimum noise figure [1–3]. Further band gap engineering of SiGe facilitates in reducing forward voltage drop of the emitter–base junction by uniform grading at the emitter–base junction without affecting the other parameters [4] which makes it a best candidate for low voltage applications in wireless phones and other low power battery operated products. In addition to allowing very complex custom designs, high speed and high breakdown voltage SiGe heterojunction bipolar transistors (HBTs) can be merged with high density CMOS using a mixed signal ASIC methodology or other CMOS macros such as micro controllers and embedded SRAM.

The primary motivation for a SiGe based HBT technology is the ability to merge the high performance SiGe HBT with standard CMOS technology giving rise to a high performance SiGe BiCMOS process without compromising the performance of the HBT or CMOS device. The combination of SiGe HBTs with scaled BiCMOS to form SiGe HBT BiCMOS technology presents an exciting possibility for system–on–chip (SoC) solutions. Further, the use of SiGe devices allows many new functions to be added onto the silicon chip thus potentially reducing cost and power and increasing speed and yield. Ge–ion implantation into silicon has been successfully demonstrated to form SiGe [5–6]. But, it is difficult to obtain shallow junctions with

sharp impurity profiles in vertical structures. However, recently it has been shown that this technique can be attractive for lateral SOI HBT [7].

The main requirement for the analog and mixed signal circuit designer is to have high speed and high current−driving PNP bipolar transistor comparable to that of NPN transistor in applications such as complementary (npn/pnp) bipolar technology and particularly in push−pull amplifier designs. However, PNP transistors have poor current gain and high collector resistance due to the low hole mobility. To overcome this problem, Schottky collector (PNM) transistors have been suggested in literature [8]. But these are vertical structures and are difficult to fabricate. Recently, Kumar and Rao [9] have demonstrated that using a lateral PNM Schottky collector structure, transistors with performance better than that of lateral PNP BJTs can be realized. However, the application of SiGe to the base region of lateral PNM Schottky collector transistors has not been reported in literature so far.

The main objective of this work is therefore to explore if the performance of the lateral PNM transistor on SOI can be improved significantly using a SiGe base. We demonstrate using two−dimensional simulation [10] that a lateral PNM HBT using SiGe base exhibits excellent characteristics over the conventional equivalent lateral PNP HBT in terms of high current gain, complete elimination of Kirk effect, approximately zero storage time and high cut−off frequency. The DC and transient characteristics and a possible fabrication methodology compatible to BiCMOS technology are discussed in the following sections.

II. Device Structure and Parameters

Fig. 1 shows the top and cross−sectional view of the lateral PNM SiGe base transistor which has been implemented in the two−dimensional device simulator

ATLAS [10]. The SOI film thickness is chosen to be 0.2 μm and buried oxide thickness is 0.38 μm. The emitter length is 3.8 μm with p−type doping equal to 5 x 10^{19} cm^{-3} and the base length is 0.4 μm with n−type doping equal to 5 x 10^{17} cm^{-3}. The base region can be converted into uniform SiGe using ion−implantation [5−6]. We have assumed the Ge composition in the silicon base to be 20% which is the maximum limit in most practical applications [11−12]. The base contact is obtained using the N^+ − poly deposited on the n−base region. These parameters are exactly same as that of the SOI lateral PNM SCBT device structure [9], except the presence of the uniform SiGe in the base region. The platinum silicide Schottky contact is taken at the right edge of the base which acts as a metal collector. The barrier height for platinum silicide and n−SiGe base−collector junction is taken to be Φ_{Bn}=0.82 eV based on experimental results reported in literature [13]. The platinum silicide is chosen because of the better process selectivity and low resistivity. The SOI lateral PNP HBT, which has been used for the comparison purpose, has exactly the same dimensions, impurity concentrations and uniform base germanium composition as that of the lateral PNM HBT except that the collector doping of lateral PNP HBT is chosen to be 9 x 10^{17} cm^{-3} so that both the devices have identical collector breakdown voltage BV_{CEO}.

III. **Device Fabrication**

The fabrication of lateral BJTs on SOI has been reported in literature [9, 15−18] and a similar procedure with a slight modification can be used to fabricate the SiGe base lateral PNM transistors on SOI as illustrated in Fig. 2. We start with an SOI wafer having an epitaxial layer of thickness 0.2 μm and doping of 5 x 10^{17} cm^{-3}.

After mesa–isolation, a thick CVD oxide is deposited and patterned as shown in Fig. 2(a). Following this, a nitride film is deposited [Fig. 2(b)] and an unmasked RIE etch is performed until the planar silicon nitride is etched retaining the nitride spacer at the vertical edge of thick CVD oxide [Fig. 2(c)] [15]. Next, the P^+ emitter is formed by implanting boron at a wafer tilt angle of 15° with an implantation energy of 30 KeV at a dose of 7 x 10^{14} cm^{-2}. As verified by the process simulator ATHENA [14], the above tilt angle will ensure that there is no short between p^+ emitter region and n^+ –poly base contact. If we choose less than this tilt angle, the p^+ emitter will be too close to the n^+ –poly base contact which will result in a more base recombination current [15]. Following the p^+ emitter region formation, a thick CVD oxide is deposited [Fig. 2(d)] and CMP process is done to planarize the surface. Selective etching is used to remove the nitride spacer, which will create a window in the oxide as shown in Fig. 2(e). Germanium can be implanted through this window to convert the silicon in the base region to SiGe. It has been reported [5] that this implantation can be performed at an energy of 130 KeV and fluences of 1, 2, or 3 x 10^{16} cm^{-2}. To re–crystalize the implanted SiGe layer, rapid thermal annealing (RTA) is performed at 1000° C for 10 s. This process will ensure complete re–crystallization of amorphous layer [5]. After depositing in situ n^+ – poly into the implanted window, the wafer is once again planarized using CMP leaving n^+ – poly in the place where the nitride film was present [Fig. 2(f)]. Now a mask is used for etching both the field oxide and the silicon film to open a contact window for the Schottky metal collector as shown in Fig. 2(g). Using another mask, the p^+ emitter contact window is opened by etching the field oxide. Following this, platinum silicide is deposited and patterned to form the Schottky collector contact and ohmic contacts on the emitter and n^+ – poly base region. The final structure is as shown in Fig. 1(b).

IV. Simulation and Discussion of Results

To understand the DC and transient characteristics of proposed lateral SiGe base PNM HBT, we have used the two−dimensional simulator ATLAS [10]. Drift−diffusion calculations are carried out using appropriate physical models. The concentration dependent mobility, field dependent mobility, and Klassens mobility models are used and the band gap narrowing effect is taken into account [11−12]. Carrier statistics are performed by defining Fermi dirac distribution and minority carrier lifetime including the effect of Shockley−Read−Hall and Auger recombination mechanisms [20]. To account for the Schottky junction property, the standard thermionic emission model is used incorporating the effect of image force barrier lowering phenomenon [21]. The unity current gain frequency f_T and the transient response are determined by performing the numerical small signal analysis. To validate the accuracy of the physical models, we have first tuned these models to precisely match the results of already published work on lateral NPN HBT on SOI [7]. The simulated DC and AC performance of the proposed PNM structure and its comparison with the lateral PNP HBT are discussed below.

(a) DC Characteristics

The output current−voltage characteristics of both the lateral SiGe base PNM and PNP HBTs are illustrated in Fig. 3. The proposed lateral PNM HBT exhibits excellent I−V characteristics in terms of high output conductance, large collector current and high transconductance g_m over conventional PNP HBT for a given base current. It may be pointed out that the PNM structure exhibits a finite off−set voltage of $V_{EC} \cong 0.2V$ which is common to any Schottky collector transistor [8] and should be considered while designing the digital logic circuits.

Fig. 4 shows the Gummel plot of both the lateral PNM and PNP HBT for a fixed collector base voltage (V_{CB}=−1V). We observe that the SiGe base PNM structure exhibits a lower base current than that of the PNP HBT due to a finite electron current caused by the electron flow from metal into the n−base when the Schottky collector junction is reverse biased. It is also seen that the collector current of the PNM HBT is more than that of the PNP HBT even at high−level injection of carriers clearly proving the absence of Kirk effect [22]. However, in the case of PNP HBT, the rapid increase in the base current at forward voltage V_{EB} >0.8V indicates the presence of strong base widening. At high−level injection, the base current rises to maintain charge−neutrality in the widened base region. This forces the base terminal to supply additional electrons leading to an increase in base current. Since the series collector resistance is governed by the doping concentration and carrier mobility in the drift region, PNM structure has a low resistivity since its collector is a metal as compared to the p− type drift collector region of the PNP HBT. This makes the Schottky collector structure immune to the base widening even at high collector currents. Further, Fig. 4 indicates that the collector current of a PNM HBT is higher than that of a PNP HBT due to the presence of the entire collector−base depletion region of the Schottky junction in the neutral base region. This decreases the effective base width, increases the injected hole gradient resulting in a higher collector current. Owing to the above two phenomenon (i. e. the reduced base current and enhanced collector current) along with better efficiency of minority carrier collection at the collector−base junction gives rise to a higher current gain in the case of PNM HBT as compared to PNP HBT as shown in Fig. 5. It is important to note that this current gain is significantly large compared to any PNP transistor reported so far in literature.

(b) Unity current gain cut−off frequency analysis.

The simulated unity current gain cut−off frequency (f_T) Vs collector current for both the lateral PNM and PNP HBT is presented in Fig. 6. The lateral PNM HBT exhibits a higher cut−off frequency, since it offers a least collector resistance and also has higher transconductance g_m compared to the PNP HBT. At a collector current of 0.2 mA, the f_T is observed to be 3.5 GHz while for the comparable PNP HBT, there is a rapid fall in f_T at this current due to the decrease in transconductance and also increased base charge storage time at high−level injection [19].

(c) Transient analysis.

The transient behavior of both PNM and PNP HBT is shown in Fig. 7 and it is clear that the PNM HBT has approximately zero base charge storage time because of the absence of base widening and a negligible minority carrier lifetime in the metal collector region. However, the PNP HBT has a higher base charge storage time not only due to the presence of the above effects but also due to the pile−up of electrons at the collector−base junction hetero−interface at high−level injection [4], [19]. Such a carrier pile−up does not seem to be present in the case of PNM structure.

V. Conclusions

In this work, for the first time, we have reported a SiGe base lateral PNM bipolar transistor on SOI suitable for non−saturating VLSI logic design. A comprehensive comparison of the lateral PNM and PNP hetero−junction bipolar transistor's steady state and transient behavior has been explored successfully using two−dimensional simulation. Based on our simulation results with uniform Ge profile, we demonstrate that the proposed lateral PNM HBT exhibits excellent

characteristics in terms of enhanced current gain, higher cut−off frequency, and fast switching response. Further a simple fabrication procedure compatible with BiCMOS process is also discussed with minimum number of masks. The proposed structure may be attractive for low power and high frequency BiCMOS VLSI applications because of the least reverse recovery time which results in not only a faster response but also negligible power dissipation during switching transitions thus minimizing the power−delay product**.**

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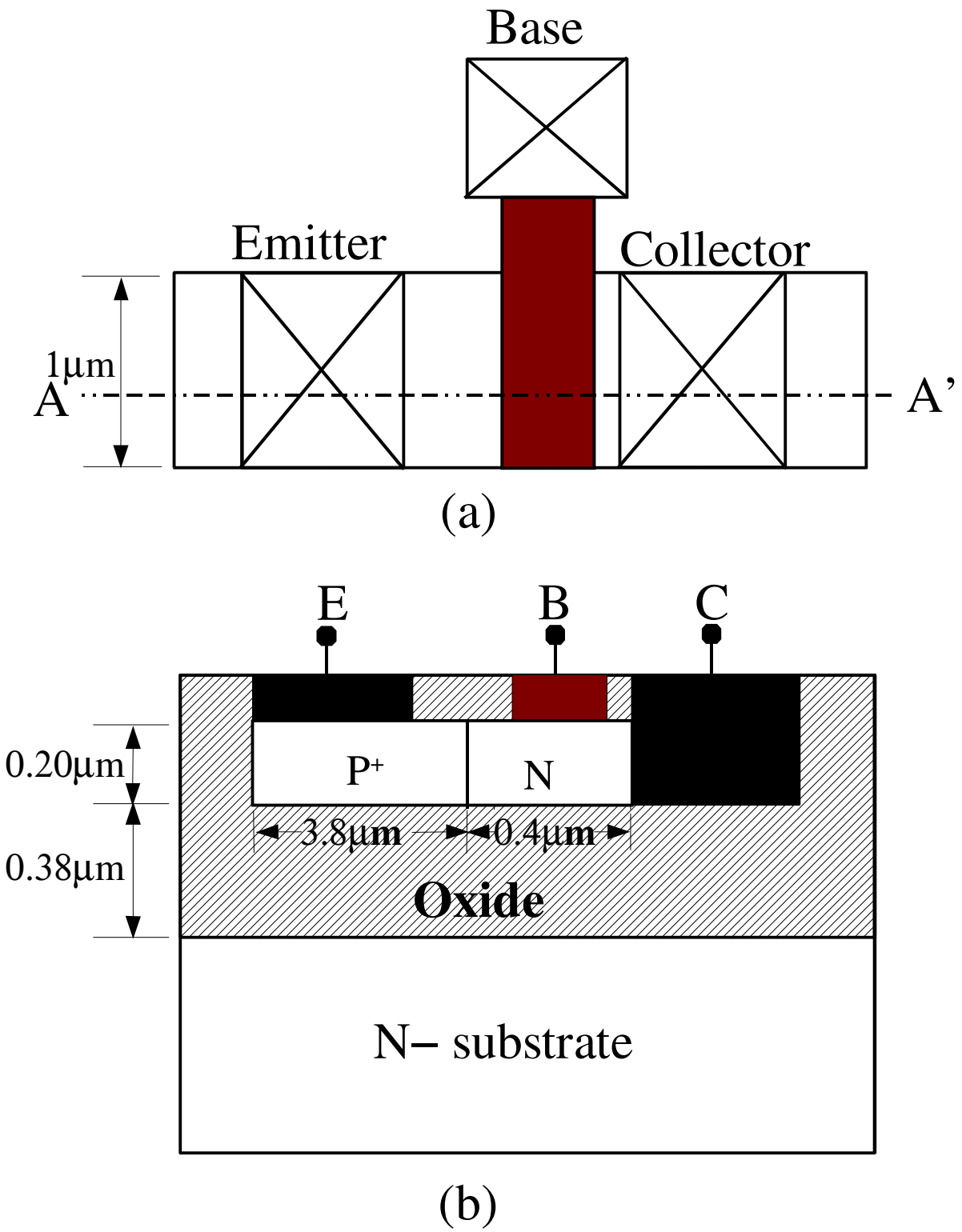

Fig. 1 Lateral PNM SiGe HBT implemented in this investigation. a) Top lay out and b) it's schematic cross–section along AA'.

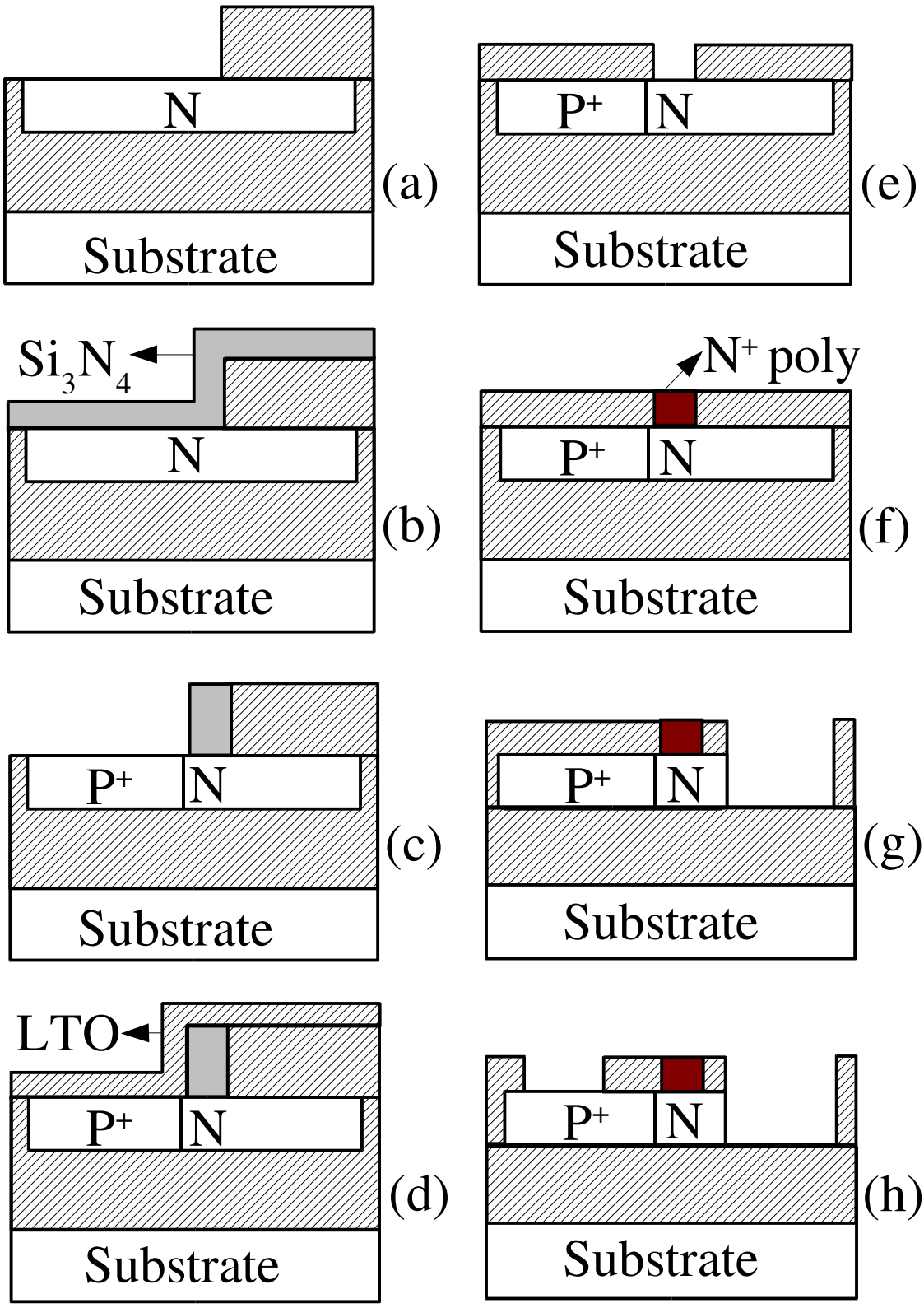

Fig. 2 Process flow for a lateral PNM SiGe HBT

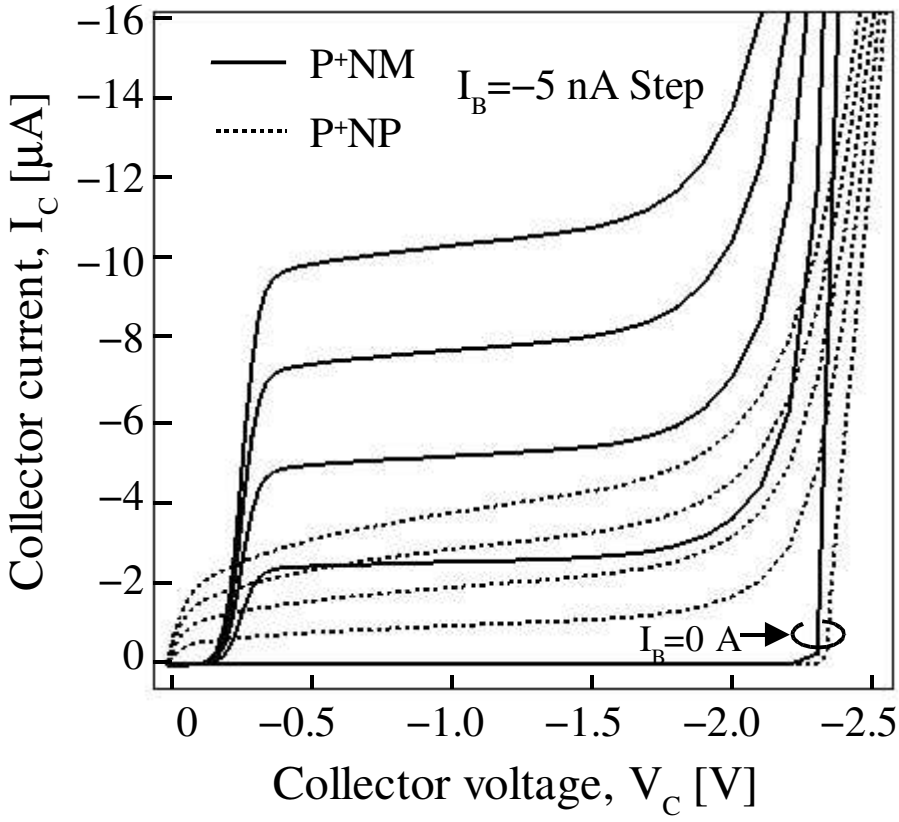

Fig. 3 Simulated common−emitter I−V characteristics of lateral PNM SiGe HBT and lateral PNP SiGe HBT structures (I_B increases from 0 to −20 nA @ −5 nA)

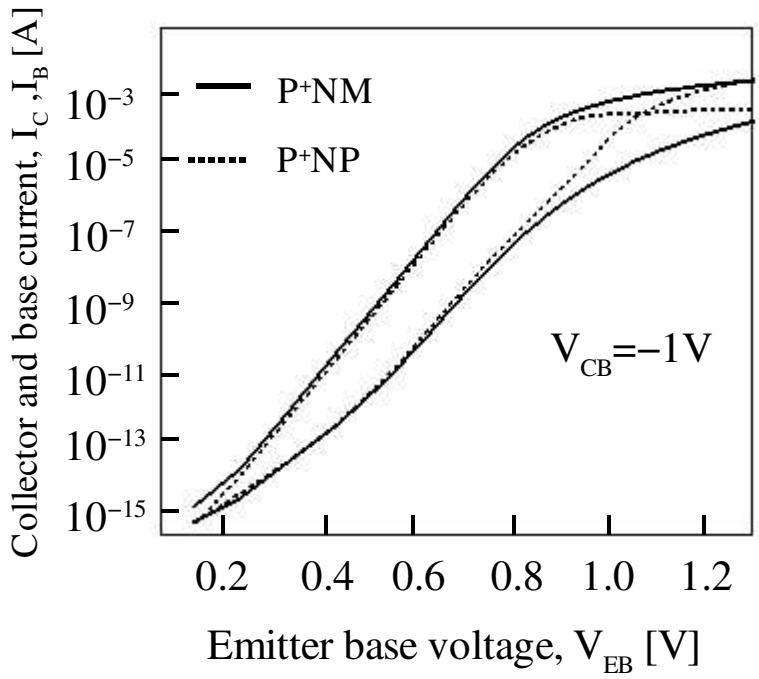

Fig. 4 Gummel plots of lateral PNM SiGe HBT and lateral PNP SiGe HBT structures

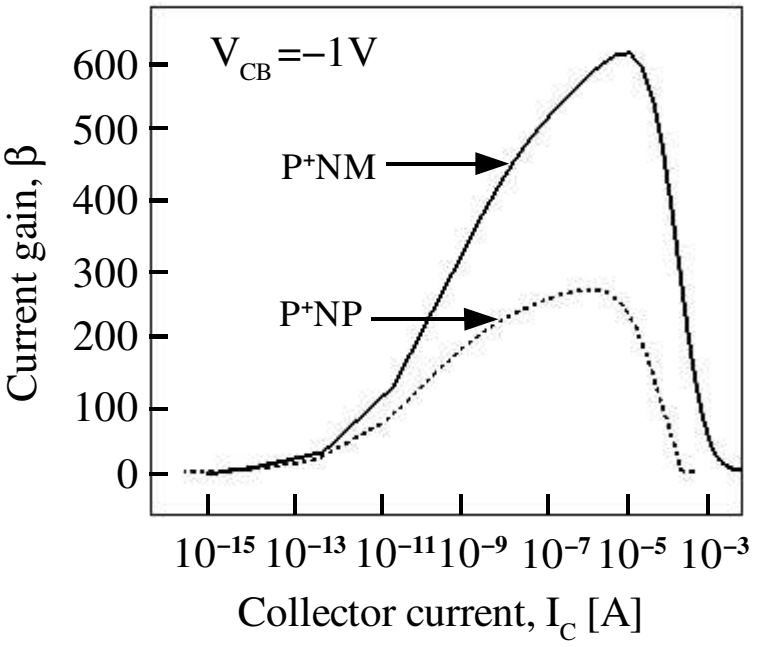

Fig. 5 Beta versus collector current of lateral PNM SiGe HBT and lateral PNP SiGe HBT structures

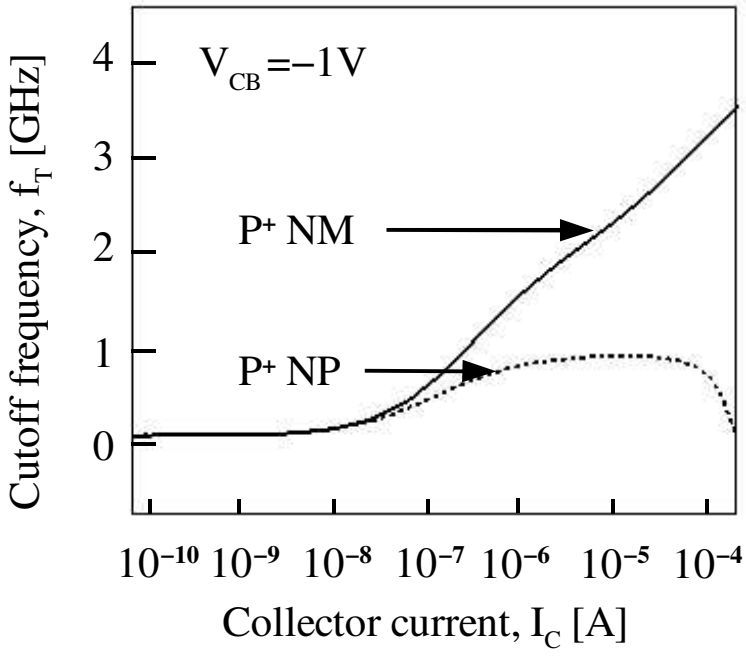

Fig. 6 Comparisons of cut off frequency performance versus collector current between lateral PNM SiGe HBT and lateral PNP SiGe HBT.

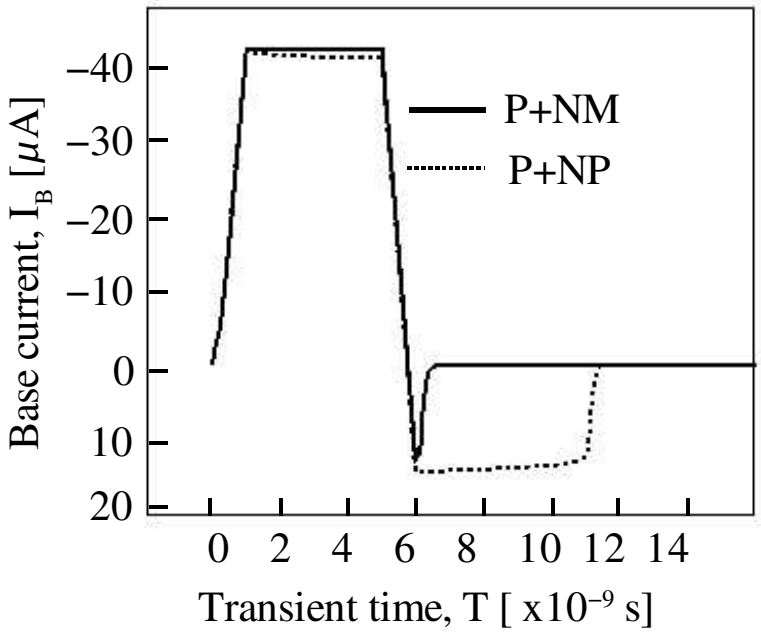

Fig. 7 Switching performance of lateral PNM SiGe HBT and lateral PNP SiGe HBT structures.