Briefs

Modeling of Voltage-Dependent Diffused Resistors

Akira Ito

Abstract— **A voltage-dependent diffused resistor model has been developed using conventional voltage controlled current sources (VCCS's) defined by a two-dimensional polynomial for simulations of mixed-signal circuits. The polynomial coefficients can be defined by a simple first-order polynomial which can be a function of geometry and process variables to accurately reflect the manufacturing process. Alternatively, a conventional junction field effect transistor (JFET) model can be used to represent voltage dependence of the diffused resistor.**

I. Introduction

BiCMOS or CMOS process technologies often provide several passive components such as polysilicon resistors, n- or p-type diffused resistors, and MOS or polysilicon/oxide/polysilicon capacitors which are essential for designing high-speed and precision mixed-signal circuits. These components also play an important role in the circuit performance and yield for mixed-signal circuits such as analog to digital converters. Most of the studies focus on the active components like MOSFET's and bipolar transistors. However, it is important to model the passive components accurately since they have voltage dependencies. Recently, several papers dealing with voltage-dependent capacitors have been published since nonlinearity is often one of the major concerns associated with switched capacitor applications; capacitor voltage dependence can be one of the significant sources of linearity error [1]–[4]. It is desirable to have fine tuned device models for passive components in addition to the active technology components. Yet resistors are generally modeled with constant values, which make high-speed and high-precision mixed-signal circuit designs difficult, time consuming, and error prone. For example, resistor ladders used in the current scaling converter circuits can be with binary weighted or R-2R type networks. The accuracy, matching, and tracking characteristics of the ladder network are dominant factors in determining the accuracy, resolution, and stability in the converters. A bandgap reference circuit operates on a known negative temperature drift of V_{BE} with a positive temperature drift of the thermal voltage V_{T} as a function of resistor ratio. Thus, the resistor sizes and sheet resistances are key factors for designing the converters. The die size depends upon the resistor size which can be unnecessarily large for mismatch and voltco considerations. The resistors can be reduced or the accuracy can be improved by using an accurate resistor model. Especially, the lightly-doped diffused resistor has a relatively high voltco which becomes a significant part of the design consideration.

To explore the design robustness, the voltage independent resistor model may not be sufficient for the mixed-signal circuit designs. In this paper, the constant resistance model has been modified to include voltage dependences as a function of geometry for the diffused resistors.

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II. Experimental

The diffused resistors used in this study were fabricated as a part of BiCMOS technology developed for mixed-signal applications [5]. Typical electrical characteristics of the n-type diffused resistor versus the applied bias are shown in Fig. 1. The resistance is for two resistor currents (I_{f}) with a P-well bias of 0 V. The diffused resistor is always reverse-biased with respect to the wells or substrate. The resistance modulates with potential difference between the resistor and well nodes. At a given current and P-well bias, the resistance of an n-type diffused resistor increases with an increase in bias. However, it is not shown here that the resistance of the p-type resistor decreases with an increase in bias. Fig. 1 clearly suggests that the voltage dependence of the resistor is due to the depletion layer spreading into the resistor. The diffused resistor should behave like a one-sided junction field effect transistor (JFET) with a very high pinchoff voltage operating in the linear region.

A typical statistical distribution of the linear voltage coefficient (VOLTCO) for a lightly-doped n-type resistor is shown in Fig. 2(a). The voltage coefficients in this paper are defined by slope/resistance. The slope is given by a linear regression of the resistance, $(V_+ - V_-)/I_{\mathrm{f}}$ versus $(V_+ + V_-)/2$ for a given N-well or P-well bias V_0. I_{f} is a forced current through the resistor for a given voltage of V_+ and V_- is the corresponding voltage. The resistance R_0 is defined at $(V_+ + V_-)/2 = 0$ and $V_0 = 0$. There is a large variation in voltage coefficient ranging from 0.0078 to 0.0088 for the n-type resistor with width and length of 10 and 50 μm, respectively. Based upon Fig. 2(b), most of the variation is explained by the variation in sheet resistance. The rest of the variation is likely due to variability in the P-well doping profile. It should be noted here that statistical variations of voltco is comparable to the active device parameters since most of the resistors used in the design are one of the active device components such as drain/source and wells.

III. Modeling of Voltage Dependent Resistors

A. VCCS Model

A linear function of V_+, V_-, and V_0 is empirically determined to be a good choice for the voltage-dependent resistance in shown Fig. 1

$$R = R_0\left(1 + c\,\frac{V_+ + V_- - 2V_0}{2}\right). \tag{1a}$$

Also, the voltage-dependent resistance may be written as a first order voltage-dependent conductance assuming that the sum of the terms related to c is much less than 1

$$g = g_0\left(1 - c\,\frac{V_+ + V_- - 2V_0}{2}\right) \tag{1b}$$

where g_0 is equal to $1/R_0$. Similarly, one can expand (1b) for a general nonlinear resistance case. Then, the voltage-dependent resistance can be expressed in terms of nodal voltages V_+, V_-, and V_0 using a polynomial

$$\begin{aligned} g = g_0\{&1 + c_1[(V_+ - V_0) + (V_- - V_0)] \\ &+ c_2[(V_+ - V_0)^2 + (V_- - V_0)^2] + \cdots \\ &+ c_i[(V_+ - V_0)^i + (V_- - V_0)^i] \cdots \end{aligned} \tag{2}$$

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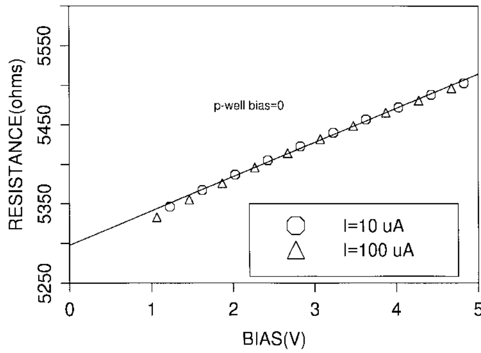
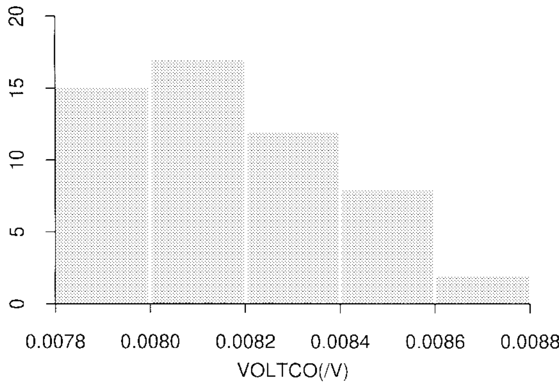
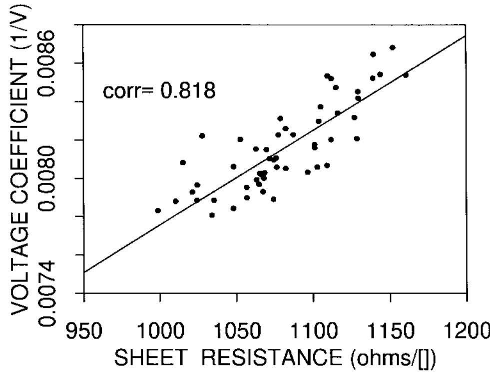


Fig. 1. Typical characteristics of the diffused lightly-doped n-type resistor with $L = 50$ μm and $W = 10$ μm.



(a)



(b)

Fig. 2. (a) Typical statistical distribution of the voltage coefficient for the n-type resistor. (b) Voltage dependence of resistors as a function of sheet resistance.

In this case, the coefficients of polynomial c_i are obtained by using a least-squares fitting routine. It should be noted here that the above equation contains a first order term of (1b).

When using Spice, the passive components can be described only as constant values. Without developing an intrinsic semiconductor device model, the resistor model can be realized by using a lumped element circuit model or JFET. This is analogous to the capacitor model [6], and DMOS model [7]. However, it is not efficient to implement a nonlinear conductance using voltage controlled voltage sources similar to the nonlinear capacitance model, since two additional equations are required to solve the nodal equations. A more efficient method is to add voltage controlled current sources (VCCS's), which can be placed between existing nodes and, therefore, demand no additional equations as shown in Fig. 3. Furthermore, two identical

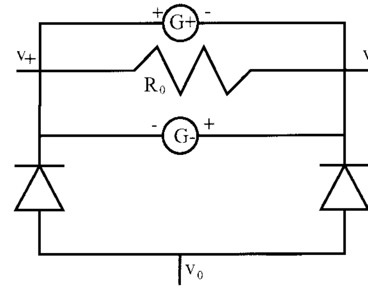


Fig. 3. An equivalent circuit model of the voltage-dependent resistor.

diodes are used to model the junction properties of the resistor. The proposed model can be expressed in terms of the current through the resistor

$$I = \frac{V_+ - V_-}{R_0} + G_+ - G_- \tag{3}$$

where G_+ and G_- are VCCS's.

In general, Spice or Spice-related circuit simulators allow the user to define VCCS's with two voltage control nodes $(V_+ - V_0)$ *or* $(V_- - V_0)$ and $(V_+ - V_-)$, which can be written

$$\begin{aligned} G_+ &= a_0 + a_1(V_+ - V_0) + a_2(V_+ - V_-) \\ &\quad + a_3(V_+ - V_0)(V_+ - V_-) + a_4(V_+ - V_0)^2 \\ &\quad + \cdots + a_i(V_+ - V_0)^j + \cdots \\ &= g_+(V_+ - V_-) \end{aligned} \tag{4}$$

and

$$\begin{aligned} G_- &= b_0 + b_1(V_- - V_0) + b_2(V_- - V_+) \\ &\quad + b_3(V_- - V_0)(V_- - V_+) + b_4(V_- - V_0)^2 \\ &\quad + \cdots + b_i(V_- - V_0)^j + \cdots \\ &= g_-(V_- - V_+) \end{aligned} \tag{5}$$

where g_+ and g_- are voltage-dependent conductances. Furthermore, the resistor must be symmetric. Therefore, the coefficients in (4) and (5) must be related as $a_i = b_i$. Substituting (4) and (5) into (3), the equation is written as

$$I = \frac{V_+ - V_-}{R_0} + g_+(V_+ - V_-) + g_-(V_+ - V_-). \tag{6}$$

Furthermore, (6) can be divided by $V_+ - V_-$ and becomes

$$g = g_0 + g_+ + g_-. \tag{7}$$

Substituting g_+ and g_- into (7), and simplifying the above equation by setting appropriate coefficients to zero based upon (2), the resistance is expressed by

$$g = g_0[1 + R_0 a_3(V_+ + V_- - 2V_0) + \cdots] \tag{8}$$

The coefficients of (8) can be determined by comparing (2) with (8). The first order term coefficient c in (1b) corresponds to the second order term coefficient $-2R_0a_3$.

B. JFET Model

JFET models in Spice contain the elements used in the VCVS model. Thus, the resistor can be modeled as a JFET. The current through the resistor can be written using the classical JFET equation

$$I_{\rm r} = \beta V_{\rm ds}[2(V_{\rm gs} - V_{\rm t0}) - V_{\rm ds}]. \tag{9}$$

Therefore, the resistance is

$$R = \frac{V_{\rm ds}}{I_{\rm r}} = \frac{1}{\beta[2(V_{\rm gs} - V_{\rm t0}) - V_{\rm ds}]}. \tag{10}$$

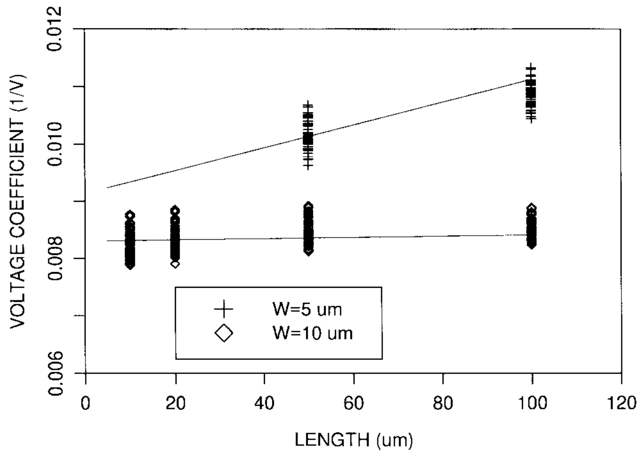


Fig. 4. Voltage coefficients of the lightly-doped n-type resistor as a function of length and width.

Simplifying the above equation

$$R = \frac{R_0}{1 + \frac{1}{2}\frac{V_{\rm ds}}{V_{\rm t0}} - \frac{V_{\rm gs}}{V_{\rm t0}}} \tag{11}$$

where R_0 is $1/-2\beta V_{\rm t0}$. For large $V_{\rm t0}$, the resistance R becomes

$$R = R_0\left(1 - \frac{1}{2}\frac{V_{\rm ds}}{V_{\rm t0}} - \frac{V_{\rm gs}}{V_{\rm t0}}\right). \tag{12}$$

Furthermore, $V_{\rm ds}$ and $V_{\rm gs}$ can be rewritten using the same notations as $V_{\rm ds} = V_+ - V_-$ and $V_{\rm gs} = V_0 - V_-$. Then, the resistance is expressed as

$$R = R_0\left(1 - \frac{1}{V_{\rm t0}}\frac{V_+ + V_- - 2V_0}{2}\right). \tag{13}$$

The voltage coefficient c in (1a) is equal to $1/V_{\rm t0}$. β and $V_{\rm t0}$ can be easily defined by c and R_0.

IV. Results and Discussion

A. Geometry Dependence

Fig. 4 shows the linear voltage coefficient c versus resistor length as a function of resistor width. The linear voltage coefficient is weakly correlated with resistor length for wide resistors, but is a strong function of resistor length for narrow resistors. The voltage across the resistor increases with length for a given current and the voltage dependence is much greater for narrow resistors than that for wide resistors due to the additional depletion layer spread along the resistor edge. Furthermore, as shown in Fig. 3, the linear voltage coefficient c has been shown to be a function of sheet resistance of the diffused resistor. Thus, it is empirically determined that c is expressed by a combination of W, L, and $R_{\rm s}$ with a reasonable accuracy based upon Figs. 2(b) and 4 [6]

$$c(W, L, R_{\rm s}) = \left(1 + \frac{d_1}{W} + d_2 L + d_3\frac{L}{W}\right)(r_1 + r_2 R_{\rm s}) \tag{14}$$

where W and L are effective width and length of the diffused resistor and $R_{\rm s}$ is sheet resistance of the diffused resistor.

Fig. 4 also shows the simulated voltage coefficients drawn by the solid lines. The coefficients $d_{i=1,2,3}$ and $r_{i=1,2}$ in (14) were determined by a regression analysis on the measured data for various combinations of the width and length.

B. Convergence Problem Associated with VCCS Model

The model must be stable under any bias conditions since the simulated voltage across the resistor can be very large before reaching

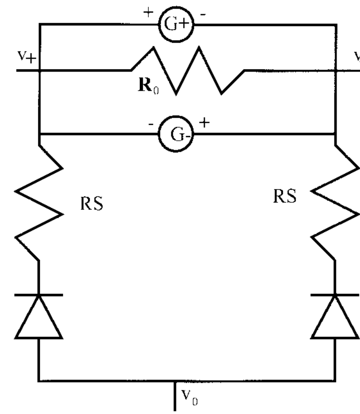


Fig. 5. An equivalent circuit model of the voltage-dependent resistor using a modified VCCS model.

a proper convergence value. When the voltage dependence term in (8) exceeds -1, the effective resistance becomes negative. In order to avoid this condition, one should add another term to the equation. The coefficient of this term should be small so that it does not perturb the resistance over the range of interest. The inclusion of the term will make the function increase or decrease monotonically. If this is not possible, one can take the diode resistance out of the diode and connect the resistance in series with the diode. Now the voltage or current controlling nodes are across the diode without the resistor. This configuration forces the voltage source to generate a voltage less than or equal to the zener voltage as shown in Fig. 5. It should be noted here that two additional nodes are required for the model, which makes the nodal equations more complicated and less efficient.

JFET model exhibits no convergence problem. It is very compact and simple to implement as a circuit model. However, the model loses a capability to simulate resistor noise properly.

In summary, it has been demonstrated that the dependence of the diffused resistor on voltage can be modeled as a lumped circuit using the VCCS or JFET models.

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"Depletion Isolation Effect" of Surrounding Gate Transistors

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***Abstract*—Sub-half-micron surrounding gate transistors (SGT's) were fabricated and their current–voltage ($I-V$) characteristics were investigated. Even in a SGT whose Si pillar is not fully depleted (e.g., 0.6 μm SGT), by using the lower diffusion layer of the Si pillar as drain and applying sufficiently high voltage, $I-V$ characteristics inherent to fully-depleted devices (i.e., subthreshold swing as low as 60 mV/dec., lowered threshold voltage independent of substrate bias voltage) were observed ("depletion isolation effect").**

I. Introduction

Much attention has been paid to surrounding gate transistors (SGT's) due to their structure (Fig. 1). Since an SGT is a vertical transistor utilizing a Si pillar as its body with a gate polysilicon surrounding the body [1], [3]–[5], it can be arranged in dense, cross-point-type memory cell arrays. First, an SGT DRAM cell was proposed [2], and after a demonstration of an SGT DRAM gain cell [6], nonvolatile memory cells have been proposed by two groups [7], [8]. However electrical characteristics of SGT's were not fully described.

This brief describes the current–voltage (I$-V$) characteristics of SGT transistors with a half-micron feature size. It was found that, by using the lower diffusion layer of the Si pillar as drain and applying sufficiently high voltage, $I-V$ characteristics inherent to fully-depleted devices (i.e., subthreshold swing as low as 60 mV/dec., lowered threshold voltage independent of substrate bias voltage were observed ("depletion isolation effect") even in nonfully-depleted (e.g. 0.6 μm) SGT's.

II. Device Fabrication

Conventional CMOS twin tub processes were used for sample device fabrication. Si pillars were formed by conventional reactive ion etching technique. Impurity concentration in the Si pillar was about 5×10^{16} cm^{-3}. Si pillar height was about 1 μm and gate oxide thickness was 10 nm. Phosphorus-doped N^{+} polysilicon was used as a gate conductor. Source and drain diffusion layers were formed by As^{+} and B^{+} ion implantation for Nch and Pch SGT's, respectively. Following the contact hole formation, Al–Si–Cu layer was formed and patterned as wiring layer to diffusion layers.

III. Results and Discussion

Fig. 2 shows the $I_{\rm D}$–$V_{\rm G}$ and the $I_{\rm SUB}$–$V_{\rm G}$ characteristics of a 0.6-μm Nch SGT, in which the Si body is not fully depleted. In Fig. 2(a) drain voltage was selected to be 2 V, and in Fig. 2(b) it was 3.5 V. Substrate bias voltage was selected to be 0, -1, and -2 V in both cases. $I-V$ characteristics both in the case when lower diffusion layer (LDL) was used as source and in the case when LDL was used as drain are shown in the same figures. It is clear that, by interchanging source and drain, the $I-V$ characteristics changed significantly in the case of high drain voltage ($V_{\rm D} = 3.5$ V). $V_{\rm th}$ becomes lower and subthreshold swing becomes steeper when LDL is used as drain compared with those when LDL is used as source. On the other hand, they scarcely changed in the case of low drain voltage ($V_{\rm D} = 2$ V).

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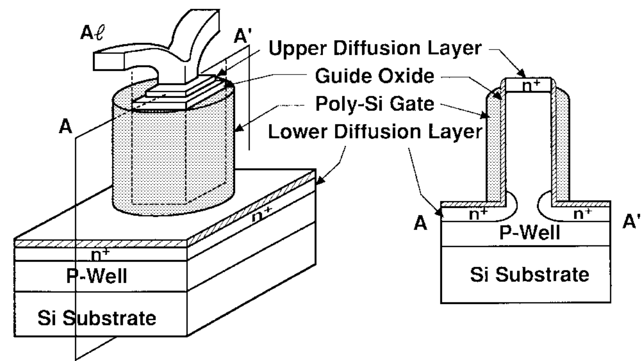

Fig. 1. Schematic view of surrounding gate transistor (SGT) structure.

In the case of low drain voltage, the maximum substrate current, $I_{\rm SUBmax}$, is smaller when LDL is used as source. In the case of high drain voltage, however, when LDL is used as source, $I_{\rm SUBmax}$ is larger than when LDL is used as drain. Similar changes in characteristics were observed in a 0.6-μm Pch SGT, in which the Si body is also not fully depleted. Fig. 3 shows the drain voltage dependence of the $I_{\rm D}$–$V_{\rm G}$ characteristics of a 0.6-μm Pch SGT, where LDL was used as drain. Drain voltage was chosen to be -2.5, -3.5, and -4.5 V. Substrate bias voltage was selected to be 0, 1, and 2 V for all cases. $V_{\rm th}$ variation due to the change in substrate bias voltage disappeared in the case of $V_{\rm D} = -4.5$ V.

The above-mentioned phenomena show that, even in both Nch and Pch SGT's in whose Si bodies are not fully depleted, by using LDL as drain and applying "high" drain voltage, $I-V$ characteristics inherent to the fully-depleted devices (i.e., subthreshold swing as low as 60 mV/dec., lowered threshold voltage independent of substrate bias voltage) can be observed.

Fig. 4 shows the schematic explanation for the above phenomena. The depletion layer extends from the LDL edge toward the center of the Si pillar by the drain voltage applied to LDL. When drain voltage becomes large enough, the inner region of the Si pillar becomes electrically isolated from the substrate by the depletion layer extending from the LDL edge. Then the potential of the inner region of Si pillar becomes immune to the substrate bias voltage. It is floating from the substrate ("depletion isolation effect"). Therefore, the surface potential of the channel region is controlled completely by the gate voltage, resulting in the above-mentioned characteristics.

The evidence that the inner region of the Si pillar is electrically isolated from the substrate is found in the polarity dependence of the $I_{\rm SUB}$–$V_{\rm G}$ characteristics shown in Fig. 2. In the case of low drain voltage, the amount of $I_{\rm SUBmax}$ is larger when LDL is used as drain, since the carrier generation region due to impact ionization is closer to the substrate contact. In the case of high drain voltage, however, $I_{\rm SUBmax}$ is smaller when LDL is used as drain. This is presumably due to the decrease in the electric field in the depletion region near the LDL edge. This decrease indicates the change in potential in the nondepleted region, which implies that the nondepleted region is floating from the substrate.

Although the above-mentioned $I-V$ characteristics can be also observed in other nonfully-depleted devices such as partially-depleted

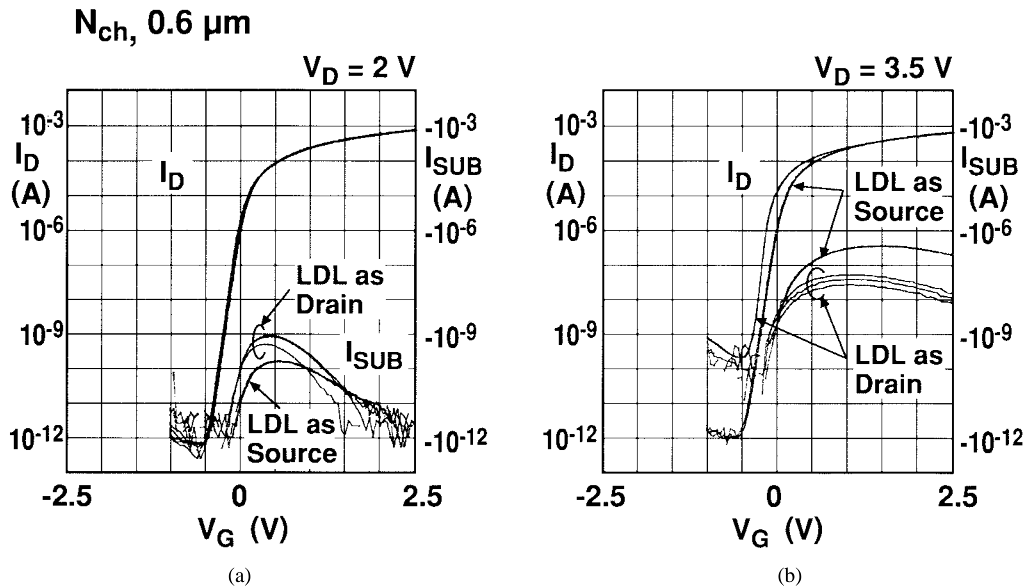

Fig. 2. The I_D–V_G and the I_{SUB}–V_G characteristics of a 0.6-μm Nch SGT, in which the Si body is not fully depleted. (a) Drain voltage, V_D, was selected to be 2 V. (b) V_D was 3.5 V. Substrate bias voltage was selected to be 0, −1, and −2 V in both cases. $I-V$ characteristics both in the case when LDL was used as source and the case when LDL was used as drain are shown.

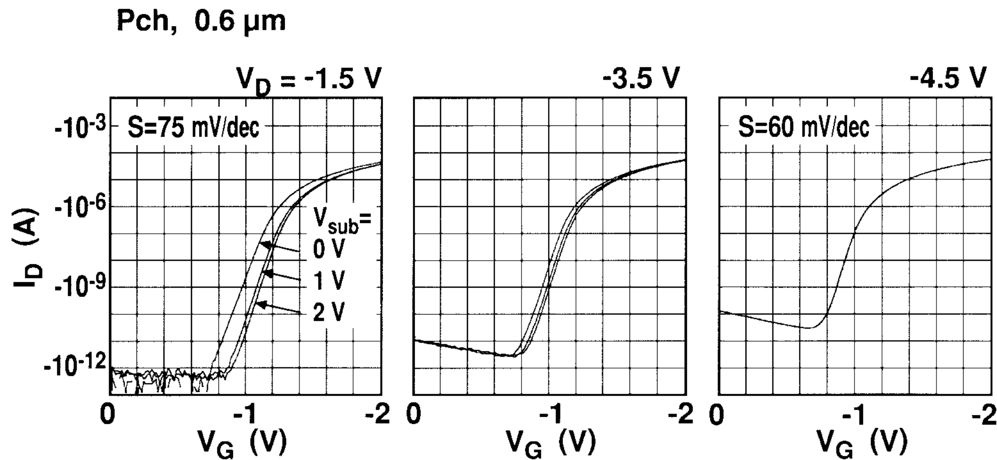

Fig. 3. Drain voltage dependence of the I_D–V_G characteristics of a 0.6-μm Pch SGT, where LDL was used as drain. V_D was chosen to be −2.5, −3.5, and −4.5 V. Substrate bias voltage was selected to be 0, 1, and 2 V for all cases.

(PD) SOI transistors under high drain bias voltage, those observed in SGT have a distinct difference from those in PD SOI transistors. As shown in Fig. 2, even in the case of "depletion isolation," substrate current, I_{SUB}, still flows in SGT. This substrate current is considered to sweep away the excess majority carriers in the Si body, reducing the base current (i.e., hole current injected into the source region) of the parasitic bipolar transistor. This means that the floating-body effect is mitigated in SGT's compared with PD SOI devices without body terminals.

The mechanism of I_{SUB} generation in the case of "depletion isolation" can be explained as follows. First, the majority carriers generated by impact ionization near drain region accumulate in the nondepleted region within Si pillar. Then the potential of the nondepleted region rises. There is a "saddle point" of the potential along the symmetrical axis of Si pillar near LDL edge, because the depletion layer extends from LDL edge toward the center of Si pillar. Thus the increase in potential of the nondepleted region stops after it reaches the level of the "saddle point," since the excess carriers are able to flow out.

It is expected that, when LDL is used as drain, the drain voltage affects the $I-V$ characteristics of SGT in which the Si pillar is not fully depleted. This effect in $I-V$ characteristics is clearly seen from the I_D–V_D curves, as shown in Fig. 5. Fig. 5 shows the I_D–V_D characteristics of Pch SGT's with the Si pillar size of 0.4, 0.6, and 1.2 μm, where LDL was used as drain. Small "kinks" in the I_D–V_D curves due to "depletion isolation effect" were observed only in SGT of the 0.6-μm pillar size. In larger SGT, the nondepleted region within the Si pillar does not become floating in the range of drain voltage used. This situation is similar to the case of a PD SOI device with a body terminal. In smaller SGT, because the Si pillar is fully depleted as is the case of a fully-depleted SOI device, no kink is apparent in Fig. 5.

IV. Conclusion

$I-V$ characteristics of miniaturized SGT's were investigated. It was found that "depletion isolation" occurs in nonfully-depleted SGT's where the lower diffusion layer is used as drain and applying sufficiently high voltage. It was also found that the substrate current

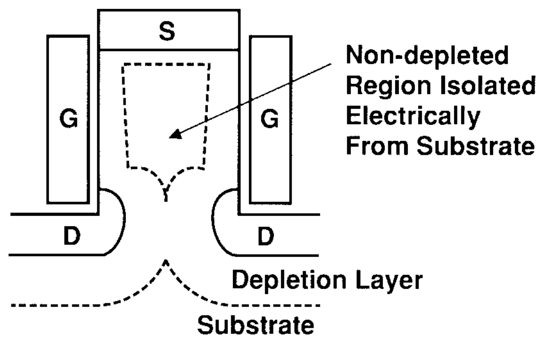

Fig. 4. Schematic cross-sectional view of a SGT operated in the "depletion isolation" mode. Dashed curve represents the depletion layer edge. Because the inner region of the Si pillar is electrically isolated from the substrate, its potential is immune to the substrate voltage.

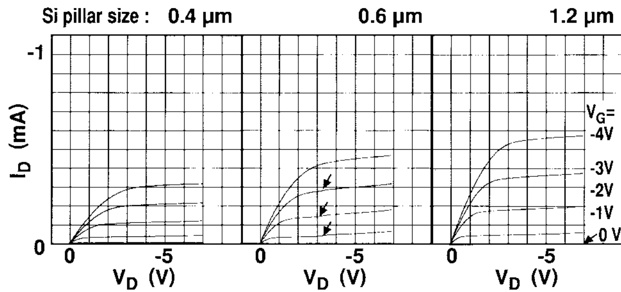

Fig. 5. I_D–V_D characteristics of Pch SGT's with the Si pillar size of 0.4, 0.6, and 1.2 μm, where LDL was used as drain.

still flows out even tin the depletion isolation operation. This is one of the major differences between nonfully-depleted SGT's and PD thin-film SOI devices, which mitigates the floating-body effect in SGT's.

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Miller's Approximation in VLSI and Power Bipolar Transistors with Reach-Through Collectors

M. Jagadesh Kumar and Krishanu Datta

***Abstract*—Using a modified ionization model based on nonlocal impact ionization, Miller's relationship is examined for typical reach-through collector VLSI bipolar transistors with collector epi-thickness between 0.025 and 1 μm. The empirical parameter n in Miller's relationship is evaluated under nonlocal impact ionization conditions within the useful range of current gain which corresponds to $0.1 > 1 - 1/M > 0.005$. The validity of Miller's relationship is also examined for power bipolar transistors having reach-through collectors ($W_{\rm epi} \leq W_{\rm pt}$) using local ionization model and design curves for the empirical parameter n are provided for different collector structures.**

I. Introduction

Although reach-through collector structures are of great importance in improving the performance limits of both VLSI and power bipolar transistors [1], [2], an interesting question which so far has received no serious attention is examining the validity of Miller's approximation in these structures. To the best of our knowledge, the applicability of Miller's approximation for reach-through structures has not been studied in literature. The aim of the present paper is therefore to evaluate the avalanche multiplication factor M using numerical simulation in reach-through collector VLSI and power bipolar transistors and estimate the empirical parameter n in Miller's approximation for different reach-through collector structures.

Miller [3] proposed a simple empirical relationship for M and is given by

$$M = \frac{1}{1 - \left(\frac{BV_{\rm ceo}}{BV_{\rm cbo}}\right)^n} \tag{1}$$

where $BV_{\rm ceo}$ is the common emitter breakdown voltage, $BV_{\rm cbo}$ is the collector–base breakdown voltage, M is the avalanche multiplication factor, and n is the empirical parameter. The above approximation is still popular [4] because it gives the value of M with reasonable accuracy.

For very narrow reach-through collector structures used in VLSI transistors, it is necessary to consider nonlocal property of avalanche

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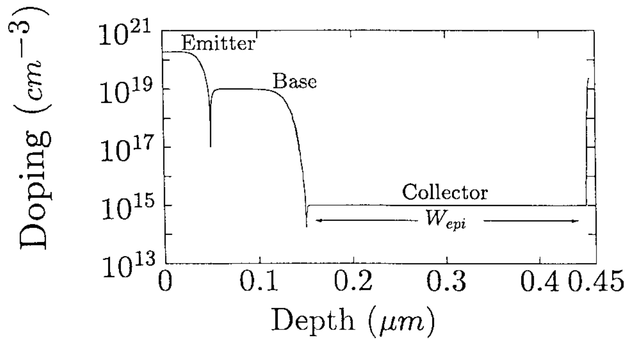

Fig. 1. Schematic diagram of the doping profile used in the simulation.

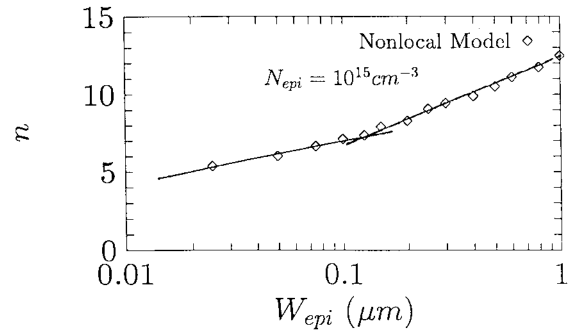

Fig. 2. The value of n as a function of collector epi-layer thickness obtained using nonlocal ionization model.

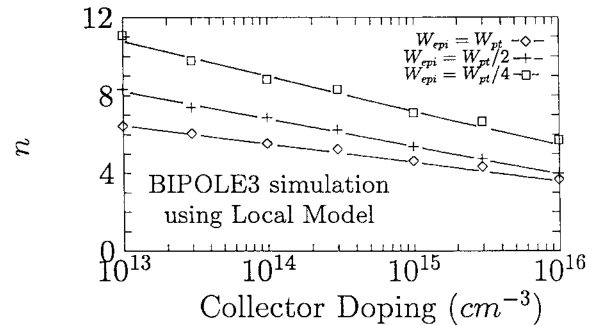

Fig. 3. The value of n as a function of collector doping obtained using local ionization model.

multiplication [1], [5], [6] to evaluate M. However, in reach-through collector power bipolar transistors, the collector depletion region width can be several microns long and hence it is necessary to use local avalanche multiplication model [7] to evaluate M in such structures.

II. Simulation Results and Discussion

We have used standard ionization rates for the local model [7] for the reach-through collector power transistors and the published data on ionization coefficients by Marsland [8] with $\lambda_w = 55.3$ nm [4] for the reach-through collector VLSI bipolar transistors. We have used BIPOLE3 device simulator [9] to estimate the multiplication factor M by numerically integrating the ionization integral (S_E) from electric field solution to Poisson's equation. All our simulations are based on the theoretical one dimensional breakdown value which does not include the sidewall breakdown or high current effects.

For simulation purpose we have taken a typical poly-silicon transistor with the doping profile as shown in Fig. 1. To verify if the Miller's approximaton for M is valid when the collector is extremely thin, we have estimated the normalized breakdown voltage as a function of $(1 - 1/M)$ for different $W_{\rm epi}$. We have observed that, within the range of $0.1 > (1 - 1/M) > 0.005$ which corresponds to the useful range of current gain $(10 < \beta < 200)$ the logarithmic plot of $(1-1/M)$ versus the normalized breakdown voltage $(BV_{\rm ceo}/BV_{\rm cbo})$ is a straight line. The value of n obtained by calculating the slope of this straight line is shown in Fig. 2 as a function of $W_{\rm epi}$. Now we have to establish up to what values of $W_{\rm epi}$, the nonlocal ionization model can be used. We notice in [1] that for a typical β (say 100), the breakdown voltage $BV_{\rm ceo}$ obtained using nonlocal model for a transistor with $N_{\rm epi} \geq 10^{17}/{\rm cm}^3$ is same as that of a reach-through collector structure with $W_{\rm epi} \leq 0.1$ μm. Hence, we infer that up to $W_{\rm epi} = 0.1$ μm, nonlocal model is clearly valid for a reach-through collector transistor. However, we need to find if nonlocal model can be used for $W_{\rm epi} > 0.1$ μm. As shown in Fig. 2, the slope of n versus $W_{\rm epi}$ changes considerably for $W_{\rm epi} > 0.1$ μm indicating that this does not fall in the nonlocal impact ionization region. However, for collector dopings $\leq 10^{16}/{\rm cm}^3$ (which corresponds to $W_{\rm epi} > 1.0$ μm), local model of impact ionization can be used with certainty [7]. To study the validity of Miller's relationship for power bipolar transistors where $W_{\rm epi} \leq W_{\rm pt}$, we have used the local impact ionization model [7] and estimated M using BIPOLE3. From the logarithmic plot of $(1-1/M)$ versus the normalized breakdown voltage $(BV_{\rm ceo}/BV_{\rm cbo})$, which is a straight line, we have estimated the value of n in Miller's relationship as a function of collector doping for $W_{\rm epi} = W_{\rm pt}$, $W_{\rm epi} = W_{\rm pt}/2$, and $W_{\rm epi} = W_{\rm pt}/4$ as shown in Fig. 3.

III. Conclusions

For the first time, we have reported the validity of Miller's approximation in both VLSI and power bipolar transistors having reach-through collectors. We have estimated the value of empirical parameter n in Miller's approximation for the above cases and provided the design curves for n.

Acknowledgment

The authors wish to thank the reviewers for their useful suggestions.

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Degradation of Tunnel-Thin Silicon Dioxide Films

I. V. Grekhov, A. F. Shulekin, and M. I. Vexler

***Abstract*—The transition of a charge transport mechanism in ultrathin (2–3 nm) SiO_2 films from Fowler–Nordheim injection to direct tunneling was found to result in the enhancement of a charge-to-degradation from $\sim 10^3$ to $\sim 10^7$ C/cm^2. Tunnel MOS structures were examined at high current density (200–1000 A/cm^2).**

I. Introduction

Today, the application of MOS structures with tunnel-thin ($d \sim 1.5$–3 nm) silicon dioxide (SiO_2) layer becomes quite realistic. Recently, such layers were successfully used in MOSFET's ($d = 1.5$ nm [1]). They may also be exploited in heteroinjectors for tunnel MOS emitter transistors [2], [3], and thyristors [4].

Nevertheless, the reliability of tunnel MOS devices has been put attention only in a few papers (for ex., [5]). There is no data on degradation of tunnel oxides in the current range of $\sim 10^2$–10^3 A/cm^2.

Summarizing the results of previous work [6], [7] one may suggest that the oxide wearout should be dramatically reduced with the change of carrier transport mechanism from Fowler–Nordheim (FN) injection to direct tunneling (DT). In other words, for any MOS structure, there should be some threshold values of a current density $j = j_c$, total voltage $V = V_c$ across the entire MOS structure and insulator voltage drop $U = U_c$ corresponding to a rapid improvement of its reliability. For example, such a feature of thin oxides was observed in [6] for the structures with $d = 3$–4 nm at low current density ($j \leq 1$ A/cm^2).

The study of the wearout of tunnel-thin SiO_2 films aims the determination of above critical values (U_c, j_c, V_c) for different types of structures and different operation modes. In this paper, we will try to find these values for tunnel MOS structures ($d = 2$–3 nm) exploited as tunnel emitters and the charge-to-degradation Q_D (i.e., the charge whose transportation results in degradation of SiO_2 film) for such structures passed by the current of 10^2–10^3 A/cm^2.

II. Concepts of Experimental Study of Degradation of Tunnel-Thin SiO_2 Films. Sample Fabrication

We examined Al/tunnel-thin SiO_2/epi–n-Si/p$^+$-Si structures [Fig. 1(a)], a positive voltage being applied to the semiconductor. Studied structure should be regarded to as to the thyristor [4] where the Al electrode is taken as an "upper" emitter, inversion hole layer (formed at the Si/SiO_2 interface) plays the role of a p-base, n-Si bulk and p$^+$-substrate are n-base and "bottom" p$^+$-emitter, respectively.

Such a device may either operate in the "active" phototransistor-like mode (at relatively low current densities) or be switched on [Fig. 1(b)], like an ordinary thyristor, into the self-maintained ON state [3] with uniform current distribution along the MOS emitter area. A conventional "thyristor's" positive feedback [4] as well as Auger (impact) ionization of Si atoms [3] (caused by *hot* electrons injected by tunnel MOS emitter) maintain the device in the ON state.

In the above-mentioned "active" mode, the magnitude of a current depends on how large is the supply of majority carriers into the bases of thyristor, especially into the inversion p-base, and on the amplification properties of "upper" (MOS) and "bottom" transistor sections. If something is happened with the oxide layer (if the degradation of SiO_2 film occurs), the current gain in tunnel MOS transistor section will decrease, because of hole leakage into the metal. Therefore, a photocurrent measured for some "standard" level of irradiation will become less.

The samples [Fig. 1(a)] were processed starting from epi–Si substrates (p$^+$-Si with $\rho = 0.005$ Ω·cm and 9-μm-thick n-Si epi-layer whose ρ is 0.3 Ω·cm). Tunnel-thin oxide films were grown in dry oxygen at $T = 700°$C during 20–40 min. An appropriate thermal contact with a heat sink had been provided so that the effect of Joule heating was not responsible for the device degradation.

III. Experimental Results and Discussion

Examined device was being kept in the ON state. From time to time, the structure was switched off for several seconds and the small-signal gain in the "active" phototransistor-like mode was checked.

The main practical result is that the reliability of investigated tunnel MOS structures may be very good so that they can be exploited in operational devices.

For example, the current flow at the level of 500 A/cm^2 resulted in noticeable degradation of the device only after 40 operating hours. Typical total electric charge whose transportation caused the changes in properties of the structure and resulted in substantial ($\sim$10%) reduction of current gain was $\sim 5 \cdot 10^7$–10^8 C/cm^2. No signs of degradation of tunnel-thin SiO_2 layer were revealed after keeping the device in the ON state for 40 h at $j = 350$ A/cm^2.

The enhancement of current density up to 700–1000 A/cm^2 greatly accelerates the degradation of devices; at 1200 A/cm^2 the operating time was never large than several seconds. In the range of 1000–1200 A/cm^2 the value of a charge whose transportation destroys the SiO_2 film reduced to $\sim 10^3$ C/cm^2, with a noticeable variation from sample to sample. This value of a charge is close to the data of [6] for "thick" oxides with FN charge transport.

Fig. 2 summarizes information on the wearout of examined tunnel structures: values of charge Q_D transported prior to a noticeable ($\sim$10%) reduction of current gain are plotted versus the current density (lower scale) and estimated insulator voltage U. The reduction of a charge-to-degradation Q_D (transition from FN to DT transport mechanism) are seen to occur within rather narrow range of current densities. Estimation of the values of electric field ε in SiO_2 layer yields $\varepsilon = \varepsilon_c \sim 10^6$ V/cm for the "critical" transition point.

When extracting the values of U, we adopted the equality of conduction band discontinuity at the Si/SiO_2 heterointerface χ_e to

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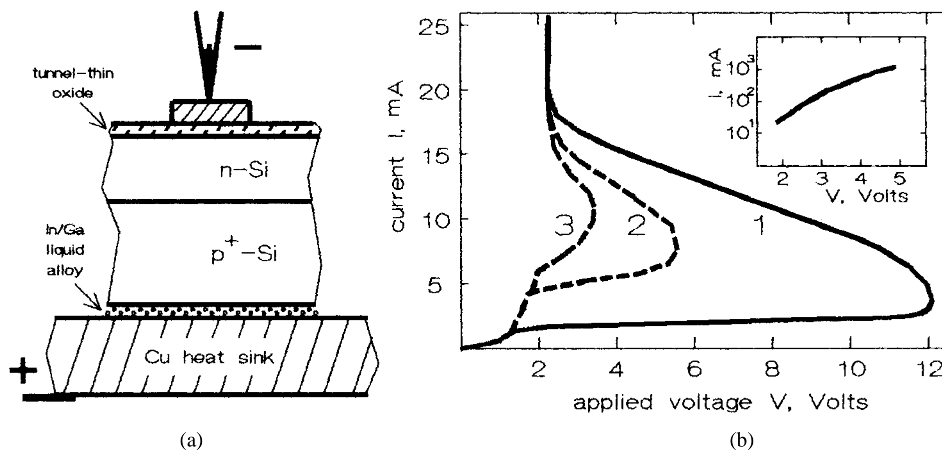

(a) (b)

Fig. 1. (a) The structure used for the study of reliability of tunnel-thin SiO_2 films and (b) typical current–voltage characteristics: 1-in a dark, 2, 3-under irradiation of different intensity, insert-device characteristic in the range of high current densities. Device area is 1.26×10^{-3} cm^2.

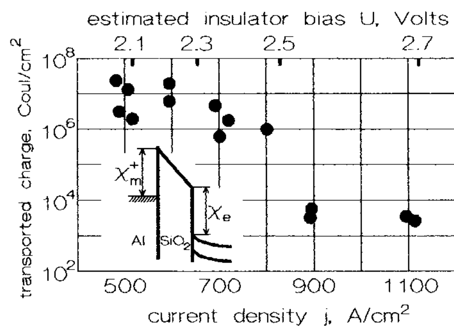

Fig. 2. Experimental results on the wearout of tunnel MOS structures (see text for details).

the metal/SiO_2 barrier height χ_m^+ (Fig. 2), as it is done in [2].

The occurrence of a *sharp* reduction of SiO_2 wearout at some $U = U_c$ offers a new way for determination of barrier heights in tunnel MOS system. Using the data of measurements, we estimated χ_m^+ as $\approx$2.5 V. This is somewhat less than the same value for "thick" MOS structures ($\sim$3.1 V) but there is nothing surprising since the barrier lowering effect may occur in the case of *tunnel* SiO_2 layer [2].

IV. Conclusion

For operation modes with DT electron transport, the charge-to-degradation Q_D measured for the *tunnel-thin* (2–3 nm) SiO_2 film is sufficiently high for device applications, namely: $Q_D \geq 10^7$ C/cm^2 at the current density j of 300–500 A/cm^2 ($j < j_c$).

DT through the 2–3-nm thick SiO_2 layers was found to be much less destructive transport mechanism than FN injection like for thicker ($\geq$ 3 nm [6]) oxides.

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Close Correspondence Between Forward Gated-Diode and Charge Pumping Currents Observed in Hot-Carrier Stressed PMOSFET's

C. H. Ling and Y. H. Goh

***Abstract*— A linear relation exists between the maximum forward gated-diode current $I_{\rm d}$ and the corresponding maximum charge pumping current $I_{\rm cp}$, in a hot-carrier stressed pMOSFET. $I_{\rm d}$ peak is further observed to shift by an amount equal to the shift in the rising edge of $I_{\rm cp}$. A close correspondence between the two currents is demonstrated.**

I. Introduction

The gate induced drain leakage (GIDL) current has been used to study hot-carrier induced interface traps, near the drain junction of MOSFET's. Much of the work done in the past has been on the n-channel device [1]–[7]. We report work on PMOSFET's, correlating the forward leakage current with charge pumping (CP) current, and providing experimental evidence for strong similarity between the two techniques.

II. Experimental

The test device was a $0.6 \times 40\ \mu{\rm m}^2$ buried-channel LDD pMOSFET, with N^+ polysilicon gate and 13.5 nm gate oxide, fabricated using a standard 0.6-μm CMOS process. The device was stressed at $V_{\rm d} = -8$ V and $V_{\rm g} = -1$ V with the source and well at 0 V. For the gated-diode measurement, the drain was forward biased at 0.25 V, with the source and well grounded. The gate bias varied from 0 to 7 V. The charge pumping current was measured using 100 kHz, 4 V peak-to-peak pulses, with the silicon surface swept from strong accumulation to strong inversion.

III. Results and Discussion

In the weakly forward bias mode, the GIDL current $I_{\rm d}$ comprises the normal (small) diode diffusion current, recombination current at bulk traps in the drain junction space charge region and recombination current at the Si–SiO_2 interface traps. Maximum recombination at the interface traps, of trap level $E_{\rm t}$, occurs when the intrinsic Fermi level $E_{\rm i}$ is midway between the electron and hole quasi-Fermi levels, i.e., $E_{\rm t}{\sim}E_{\rm i}$ and n~p. Scanning the gate bias to vary the silicon surface from accumulation to depletion, the maximum recombination condition sweeps along the channel toward the drain junction. The presence of a localized degraded region of increased interface trap density would be manifested by a GIDL current peak.

Fig. 1 plots $I_{\rm d}$ against gate bias $V_{\rm g}$, showing the evolution of the current with stress time [curves (a)–(e)]. The pre-stress current of ~1.1 pA is independent of $V_{\rm g}$, from channel accumulation to depletion. Following stress, a current peak is observed, attributed to increase in the interface trap recombination. The peak current grows in magnitude, exhibiting a logarithmic time dependence, as depicted in the inset, consistent with earlier observations [8]. The location of the current peak shifts toward higher gate bias. Electron trapping and interface trap generation are known to be the main degradation mechanisms under low $V_{\rm g}$ stress [9]. Trapped electrons over the degraded region cause the underlying silicon to invert, extending the p^- LDD drain into the channel. A higher gate bias is therefore needed to deplete the channel in the degraded region, in order for the recombination current due to the newly created interface traps to be observed.

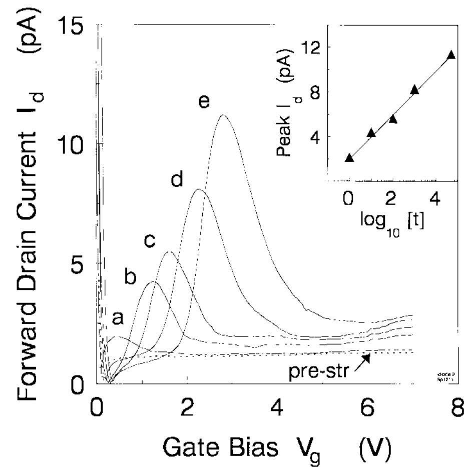

Fig. 1. Forward drain current against gate bias for stress times: (a) 1, (b) 10, (c) 10^2, (d) 10^3, and (e) 5×10^4 s. Inset shows peak current against the logarithm of stress time in s.

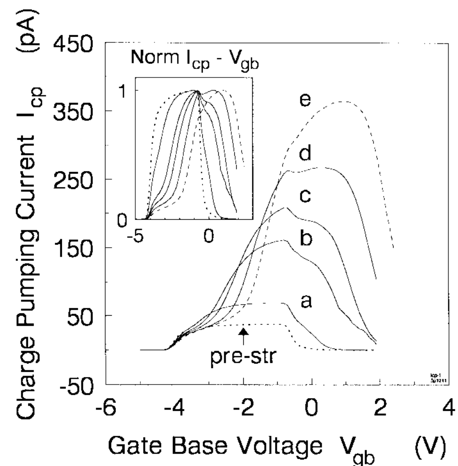

Fig. 2. Charge pumping current against gate base voltage for stress times (a)–(e) as in Fig. 1. Inset shows the normalized current.

Fig. 2 shows the corresponding charge pumping current $I_{\rm cp}$. A gradual shift in the rising edge of $I_{\rm cp}$ toward positive gate base voltage $V_{\rm gb}$ confirms trapping of negative charge. From the inset, $\Delta V_{\rm gb} \sim 2.7$ V at 0.5 $I_{\rm cp}$ (max) is measured for the maximum stress time. This gives an estimated average density of trapped charge $C_{\rm ox}\Delta V_{\rm gb}\Delta x/qL_{\rm eff} \sim 1 \times 10^{12}\ {\rm cm}^{-2}$, assuming a uniform degraded region $\Delta x \sim 0.1\ \mu$m [8], and using a measured effective channel length $L_{\rm eff} \sim 0.4\ \mu$m. The maximum $I_{\rm cp}$ is a measure of average interface trap density, which shows a 9.6 fold increase. The corresponding increase for the gated-diode current is 9.8.

To verify that the shift in the gated-diode current peak is due to drain junction extension, the device was subjected to 30 min

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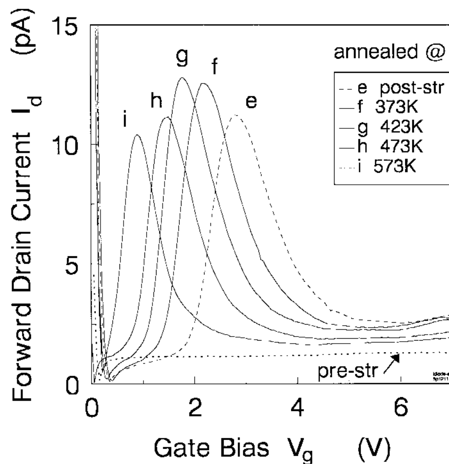

Fig. 3. Forward drain current against gate bias for pre-stress (dotted) and post-stress (dashed), and after anneal at (f) 373, (g) 423, (h) 473, and (i) 573 K.

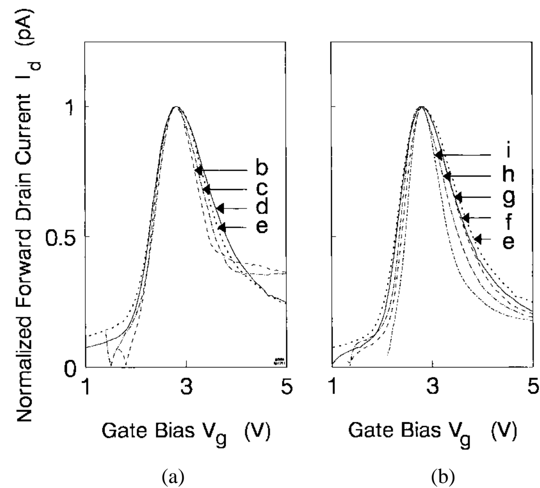

Fig. 4. Normalized forward drain current against gate bias for (a) stress times (b)–(e) as in Fig. 1 and (2) anneal temperature (e)–(i) as in Fig. 3. The curves are shifted so that the peaks coincide.

isochronal anneals over 373–573 K to detrap electrons. The current peak shifts to lower gate bias, as electrons detrap [curves (e)–(i)], as shown in Fig. 3. The GIDL current increases initially before decreasing, suggesting an initial increase in the density of the interface traps, which subsequently anneal slightly. Post-stress generation of interface traps, in particular at elevated temperatures, has been reported for NMOSFET's. The trap generation mechanism was attributed to net thermal dissociation of Si–H bonds by trapped holes and the outdiffusion of released H, which then breaks a Si–H bond at the Si–SiO_2 interface [10]. We argue that trapped holes also exist in stressed PMOSFET's, but are masked by the larger number of trapped electrons. The corresponding charge pumping currents (not shown here), show $I_{\rm cp}$(max) increasing initially and falling slightly at the highest anneal temperature. The shift in the rising edge to negative $V_{\rm gb}$ confirms detrapping of electrons.

While the GIDL peak grows with stress time, the full width at half maximum (FWHM) is relatively constant (for stress $t > 10$ s), as shown by the normalized $I_{\rm d}$ in Fig. 4(a), suggesting near spatially constant interface trap density over the degraded region. In Fig. 4(b), the FWHM is somewhat reduced at the highest anneal temperature, attributed to annealing of interface traps and the subsequent decrease in the trap density. These results demonstrate that the portion of the degraded interface, over which substantial recombination occurs, is approximately independent of the total extent Δx of the degraded region, in agreement with the sweep of a maximum recombination width along the channel with gate bias. The logarithmic growth of the GIDL current peak is attributed to recombination at bulk traps in the degraded region. The current component depends on Δx, which has been shown, from gate-drain overlap capacitance, to exhibit a logarithmic stress time dependence [8].

In the forward gated-diode configuration, gate bias is swept in a quasistatic manner. At a given $V_{\rm g}$, a constant component of the drain current feeds a steady recombination of carriers at the interface traps. For the charge pumping measurement, the gate bias pulses the channel repetitively from strong accumulation to strong inversion in a highly nonequilibrium manner. The charge pumping current is the result of carrier trapping at and emission from interface traps, over an energy interval about the midgap. The relation between forward GIDL current and CP current has been discussed [7]. Fig. 5 plots (a) maximum forward GIDL current against maximum CP current and (b) shift in GIDL current peak against shift in rising edge of CP current measured at 0.5 $I_{\rm cp}$(max), for the various stress and anneal

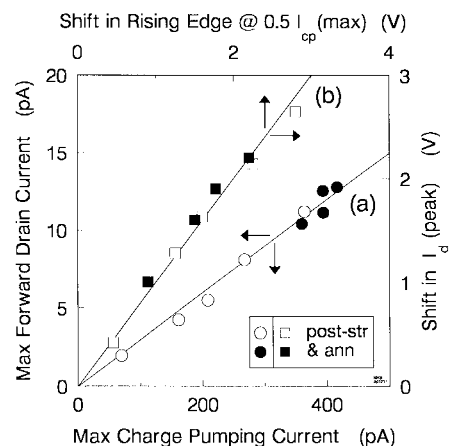

Fig. 5. (a) Maximum forward drain current against maximum charge pumping current and (b) shift in peak drain current against shift in rising edge of charge pumping current.

conditions. The straight lines provide evidence that the two currents are strongly correlated.

IV. Conclusion

We have demonstrated close correspondence between forward gated-diode current and charge pumping current and propose that the two techniques probe essentially the same interface traps. Charge pumping technique probes traps over the entire degraded region simultaneously; gated diode technique scans over the degraded region, probing only a portion of the entire region at a time.

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Investigation of the Frequency Dispersion Effect in the Root-Model Applied to Conventional and Floating-Gate MESFET's

S. Van den Bosch and L. Martens

***Abstract*—This paper investigates measurement and modeling aspects of frequency dispersion effects for GaAs MESFET s. The well-known *Root*-model's ability to simulate frequency dispersion is evaluated versus measurements. We propose an alternative frequency weighting function that can easily be implemented in the MDS[1]-system. We also investigate the validity of this approach for "floating-gate" MESFET's and present, for the first time to our knowledge, measurement results for frequency dispersion in this type of device.**

I. Introduction

The experimental modeling of active devices is an important step in the design of microwave circuits such as oscillators, mixers and power amplifiers. These nonlinear circuits typically introduce new frequency components far below typical operating or input frequencies. Accurate simulation of such circuits thus requires good knowledge and simulation of low-frequency component behavior. For GaAs MESFET's low-frequency output conductance dispersion is an important phenomenon in this respect.

The origin of frequency dispersion is generally attributed to traps in the semiconductor bulk or at the surface [1], [2]. In the past a lot of research has been dedicated to the circuit-equivalent modeling of frequency dispersion effects [3]–[6], resulting in sometimes large circuit descriptions for a single component simulation. More recently the new measurement-based modeling strategies [7]–[9] have become important. One of the best known examples of these new models is the so-called *Root*-model [7]. Although the *Root*-model allows very accurate simulation of both DC- and RF-characteristics, modeling of frequency transition effects is not quite up to the same standard. We will evaluate the errors in the *Root*-model's frequency transition simulation by comparing simulated to measured results and will propose some possible modifications.

II. Measurement and Simulation Results

A. The Root-Model

The theory of frequency dispersion in a conventional MESFET was verified through measurements performed on GaAs MESFET's with 0.7 μm gate lengths and 200, 400 (both four fingers), and 600 μm (six fingers) gate widths. At first an expression based on the *Root*-model's drain current equation was used to describe the frequency transition region (1). Three parameters, $G_{\rm low}$, $G_{\rm high}$, and τ were fitted through least-squares optimization on measured characteristics

$$G(\omega) = \frac{1}{1+\omega^2\tau^2} \cdot G_{\rm low} + \frac{\omega^2\tau^2}{1+\omega^2\tau^2} \cdot G_{\rm high}. \quad (1)$$

This is the drain current expression of the *Root*-model [7] rewritten for conductance modeling. From this equation, it can easily be seen that τ is supposed to be independent of drain-source voltage, which implies that dispersion is attributed to one particular trap level. Our measurements will show that this assumption no longer holds for even fairly moderate drain-source voltages.

Because of the inaccuracy of the *Root*-model in the transition region, we experimented with a new model leaving the exponent 2 of $\omega\tau$ in (1) as a variable real number n, determined independently of the formerly optimized $G_{\rm high}$ and $G_{\rm low}$, for each individual bias setting. We will now further investigate dispersion properties of the available MESFET's using the experimentally proposed model. For easy comparison, a percentage rms-error is defined as the root taken from the sum of all quadratic differences between measured points and (1) with exponent equal to 2 and n, respectively. This root is then divided by the value of the measured conductance thus yielding a percentage rms-error.

B. Drain-Source Bias Dependence

We first investigate the dispersive behavior of the GaAs MESFET devices under test as a function of drain-source bias. Fig. 1 shows parameters $G_{\rm low}, G_{\rm high}, f_{\rm char} = 1/(2\pi\tau)$, and $\exp = n$ as a function of $V_{\rm DS}$ for a 4×50 μm GaAs MESFET and for both the new and the old model. In addition, the earlier defined rms-error is shown. From Fig. 1 we conclude that the rms-error for the model with variable exponent is significantly smaller than for the original model. Since parameters $G_{\rm low}$ and $G_{\rm high}$ are nearly equal (as was also shown by the measurement verification), the difference is primarily situated in the transition region. Probably the most important result is that the exponent which had been left completely variable to be optimized by

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[1] Microwave Design System of Hewlett-Packard

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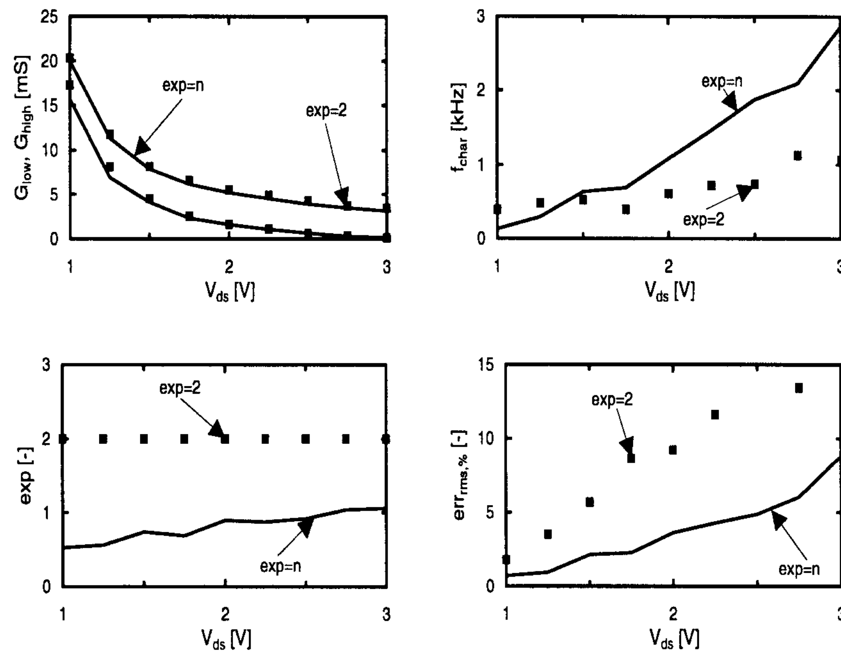

Fig. 1. Influence of bias on dispersion model parameters (G_{low}, G_{high}, f_{char}, and exp) and $\mathrm{err}_{\mathrm{rms},\%}$.

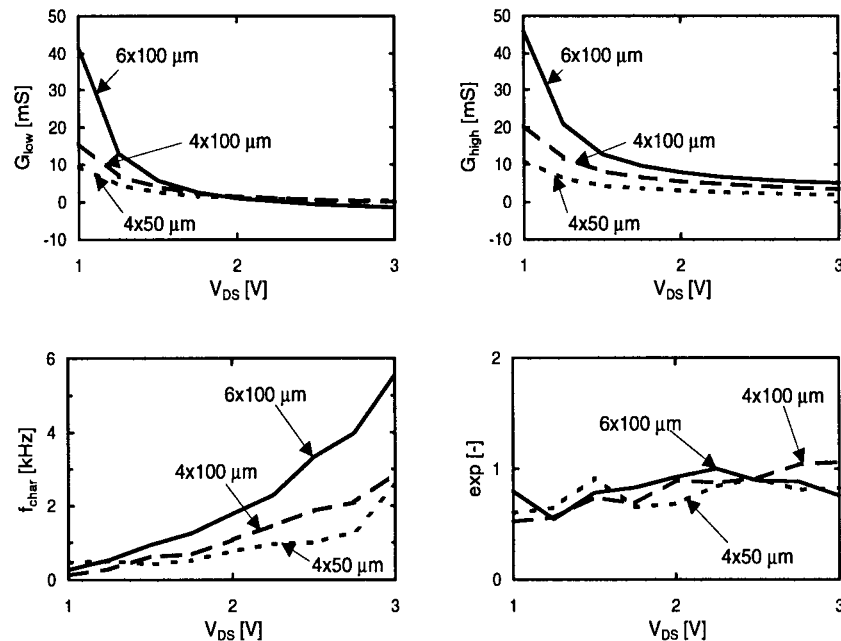

Fig. 2. Influence of device geometry on dispersion model parameters (G_{low}, G_{high}, f_{char}, and exp) and $\mathrm{err}_{\mathrm{rms},\%}$.

the least squares algorithm turns out to be nearly constant and equal to one. This result was found consistently and even more pronounced in the other MESFET's on the same wafer and thus can only be dependent on the process. The parameter τ or, in other words, the characteristic frequency f_{char}, appears to depend quite strongly on the drain-source voltage, especially at high V_{DS}.

C. Geometry Dependence

Next, we investigate the influence of device geometry on the dispersive behavior of the MESFET's. Fig. 2 shows the model parameters of three GaAs MESFET's with different geometries as a function of V_{DS}. Low-frequency output conductance G_{low} increases strongly with increasing gate width. Wider gates mean wider channels and thus lower resistance or increased conductance. Dispersion is most important for small devices and the characteristic frequency increases for larger MESFET's.

Again we find that for all device geometries the exponent is nearly constant and equal to one. For this MESFET process it is therefore easy to improve the *Root*-model's transition function. Since the characteristic frequency changes considerably with bias a correct approach would require the introduction of an additional state function for τ. However, the low frequencies at which the effect occurs and the shape of the f_{char}-characteristic suggest a nearly linear dependence on bias.

D. Floating-Gate MESFET's

One of the main problems of optimization of GaAs MESFET's for power applications is the compromise that must be made be-

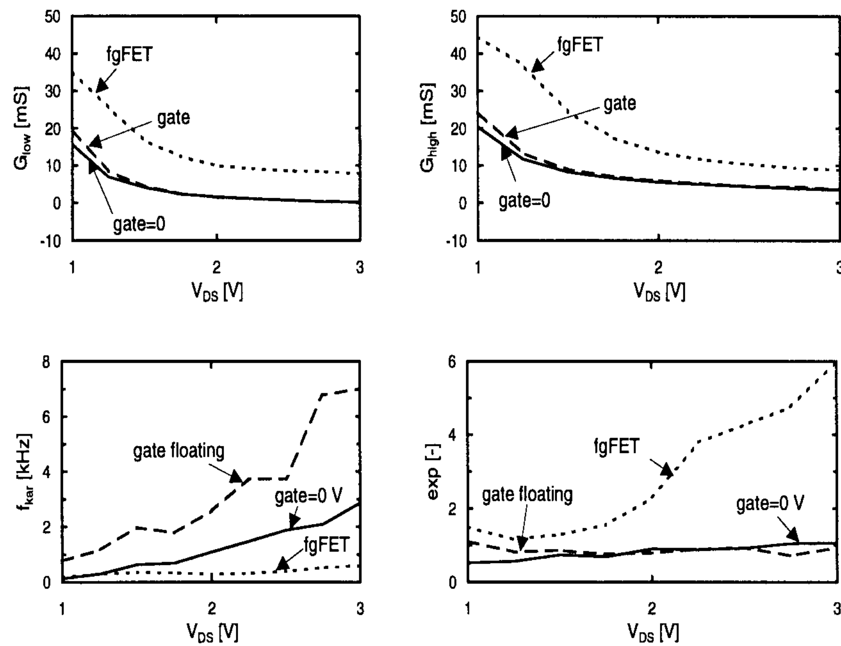

Fig. 3. Comparison of dispersion characteristics of a "floating-gate" MESFET (fgFET), a conventional MESFET with open gate (gate floating) and a conventional MESFET with $V_{\rm GS} = 0$ V (gate = 0 V).

tween high breakdown voltage $V_{\rm GD,B}$ and high transconductance G_M. An attractive alternative is offered by so-called "floating-gate" MESFET's [10]. The present paper investigates these effects using a 4 × 100 μm GaAs "floating-gate" MESFET. Results will be compared with a conventional MESFET with gate open (not probed and thus not connected) and with gate grounded (at 0 V).

Fig. 3 compares parameters extracted for a "floating-gate" MESFET with those obtained for a conventional MESFET with gate open and with $V_{\rm GS} = 0$ V. From Fig. 3, we conclude that for the same drain-source voltage $V_{\rm DS}$, $G_{\rm DS}$ is much larger for a "floating-gate" MESFET than for a conventional MESFET. This is primarily due to reduced channel reduction from the depletion region. The $G_{\rm DS}$ difference between a conventional MESFET with open gate and with $V_{\rm GS} = 0$ V is minor. The characteristic frequency is much lower for all drain-source voltages in the case of the "floating-gate" MESFET. When looking more closely at an enlarged view of the floating gate characteristic frequency versus bias one notices that it is not monotonically increasing but has dips for specific voltages. These dips are caused by the on-set of a floating gate becoming active since this occurs at regular intervals for additional floating gates becoming active. The exponent associated with the transition is not constant for "floating-gate" MESFET's as it is for conventional ones. This is probably due to the nonuniform charge distribution induced by the floating gates in contrast with the uniform depletion region with a surface charge present.

III. Conclusion

We have made a careful study of frequency dispersion effects of GaAs MESFET's. We have noticed the well-known measurement-based *Root*-model to be open for improvement and have proposed alternatives for more accurate simulation of the transition region of MESFET's of different geometries. Furthermore, we presented to our knowledge previously unpublished results for "floating-gate" MESFET's which show that these devices not only improve breakdown characteristics but also significantly alter the dispersive behavior of the component. This knowledge can be important for choosing appropriate MESFET's in for example mixer design.

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