Briefs

Separating the Influences of Neutral Base Recombination and Avalanche Breakdown on Base Current Reduction in SiGe HBT's

J. S. Hamel, *Member, IEEE*

***Abstract*—A simple experimental procedure is proposed to determine the separate ranges of reverse collector-base bias where neutral base recombination and avalanche breakdown, respectively, dominate base current reduction in silicon germanium heterojunction bipolar transistors (SiGe HBT's) which exhibit significant neutral base recombination.**

I. Introduction

A negative consequence of increased base doping and reduced bandgap in silicon germanium heterojunction bipolar transistors (SiGe HBT's) is increased neutral base recombination which has been noticed [1] even in narrow base width vertical UHV/CVD SiGe HBT's. Significant neutral base recombination leads to decreased incremental output resistance which must be accounted for in analog circuit design.

Both neutral base recombination and avalanche breakdown in the collector-base space charge layer result in changes in base current as the reverse collector-base voltage V_{cb} is altered, where base current is reduced for increasing collector-base voltage. An equivalent circuit element such as the incremental collector-base resistance r_μ [2] which models the impact of neutral base recombination on output resistance can be reliably extracted only for a range of V_{cb} where avalanche breakdown does not dominate variations in base current.

Usually a linear dependence of base current reduction on the square root of V_{cb} is assumed [3] for the range of V_{cb} where neutral base recombination dominates over avalanche breakdown. Although neutral base recombination is significant enough [4] to have a nonnegligible impact on the small signal output resistance in SiGe HBT's typical of those now in use in analog circuits, the actual reduction in base current due to neutral base recombination can be quite small for high gain devices compared to the total base current. This results in increased uncertainty in determining the precise point where avalanche breakdown will interfere with proper extraction of model parameters related to neutral base recombination. Furthermore, the linear dependence assumed by the conventional method is valid only if the collector-base space charge layer sweeps through a uniformly-doped collector that is also much lower doped than the base region such that most of V_{cb} drops across the collector portion of the collector-base space charge layer. This could have implications for devices with nonuniform collector impurity profiles resulting from collector implants to optimize high current performance or "punched through" collectors where the space charge layer encroaches on the highly nonuniform buried layer.

In this work an alternative experimental procedure is proposed which exploits the dependence of base current reduction on V_{cb} due to avalanche breakdown to determine for what V_{cb} avalanche breakdown begins to dominate over neutral base recombination. This technique has the advantage of reducing measurement uncertainty due to the larger changes in base current that occur when avalanche breakdown dominates, as well as not depending upon the assumptions regarding collector impurity profile inherent in the conventional approach. The experimental procedure is outlined in section II followed by experimental measurements using the technique on a UHV/CVD SiGe HBT in section III.

Manuscript received July 8, 1996; revised November 8, 1996. The review of this brief was arranged by Editor T. Nakamura..

J. S. Hamel is with the Department of Electronics and Computer Science, University of Southampton, Southampton, U.K.

Publisher Item Identifier S 0018-9383(97)03015-3.

II. Experimental Procedure

Instead of exploiting the linear behavior of neutral base recombination current on the square root of V_{cb}, one can also exploit the functional dependence of the avalanche breakdown current on V_{cb}. A simple derivation (see Appendix A) yields

$$V_{cb} = -BV_{cbo}\left(\frac{I_B(V_{cb}) - I_B(0)}{I_C}\right)^{1/n}. \tag{1}$$

A plot of the right hand side of (1) versus V_{cb} for the correct empirical value of n should yield a straight line for the range of V_{cb} where avalanche breakdown is dominating. The slope of such a plot will be equal to the negative of the inverse of the collector-base breakdown voltage BV_{cbo}.

III. Experimental Results

Fig. 1 shows measurements of base current versus the square root of the reverse collector-base voltage for four transistors fabricated using a UHV/CVD deposition process with nominally identical impurity profiles (Fig. 2), one being a silicon control with no Ge, and the other three having box-like Ge profiles in the base with measured peak Ge concentrations of 16%. Collector impurity concentration was doped nominally uniform 1×10^{16} cm^{-3}. The base-emitter voltage V_{be} was 0.6 V for all device measurements. Collector currents I_C at $V_{cb} = 0$ V for the silicon control, 5-nm, 10-nm, and 15-nm spacer layer SiGe devices were 4.2×10^{-7} A, 7.1×10^{-6} A, 2.6×10^{-5} A, and 2.7×10^{-5} A, respectively. All measurements were carried out on an HP 4155A parameter analyzer [5]. The process used to fabricate these devices is similar to that reported elsewhere [6] with the exception of the nominal base impurity concentration being 2×10^{19} cm^{-3} and the use of a polysilicon emitter contact. The only essential differences between the SiGe devices is the size of the undoped spacer layers used on either side of the p-doped SiGe base layer to take up boron out-diffusion. The base current has been normalized with respect to the base current at zero V_{cb}. A near linear reduction in base current in Fig. 1 before the onset of avalanche breakdown indicates that neutral base recombination is significant in the SiGe devices. Accurate determination of the demarcation between "linear" behavior and nonlinear behavior, where avalanche breakdown begins to dominate base current reduction, can be difficult using this approach since the changes in base current due to neutral base recombination compared to the total base current are quite small for these devices resulting in noisy measurements.

Fig. 3 shows measured data for the SiGe HBT with 10-nm spacer layers plotted using the above expression in (1). From the results in Fig. 3, the ranges of V_{cb} where neutral base recombination and where avalanche breakdown dominate the base current reduction can

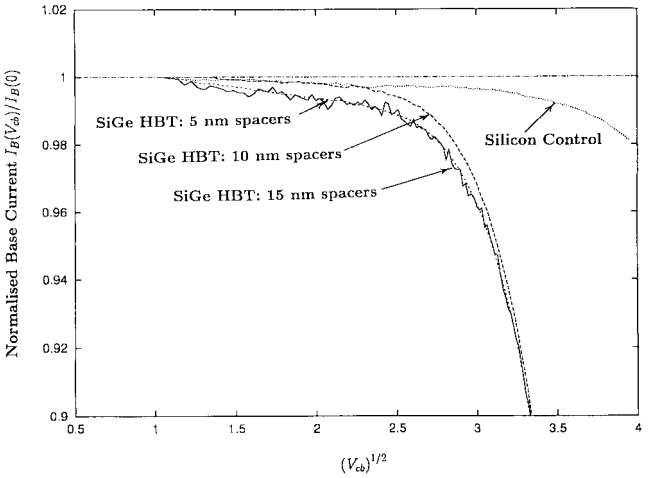

Fig. 1. Base current reduction versus the square root of the reverse collector-base voltage V_{cb} for three SiGe HBT's with different spacer layers and a silicon control. (Dotted line: silicon control, dashed lines: 5-nm and 10-nm spacer layers, solid line: 15-nm spacer layer).

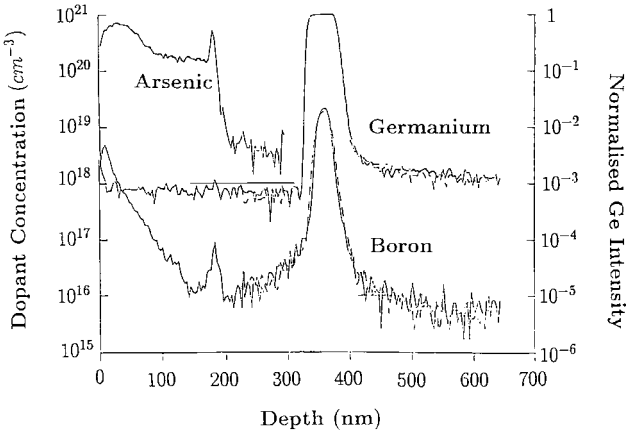

Fig. 2. Secondary ion mass spectroscopy impurity profiles of experimental SiGe HBT's and silicon control device (without Ge).

be clearly seen. A value of $n = 5$ yields a straight line, the slope of which yields a measured value of BV_{cbo} of approximately 40.0 V and a sustaining voltage BV_{ceo} of 14.7 V for a current gain of 150 using $BV_{ceo} = BV_{cbo}/\beta^{1/n}$ [7]. For this device it is found that neutral base recombination dominates the base current reduction for collector-base reverse biases below approximately 7.0 V.

From Fig. 1 it can be seen that the amount of base current reduction due to decreasing neutral base recombination varies considerably between the various the device structures. Detailed measurements of output resistance [4] have revealed that the SiGe devices with 5- and 10-nm undoped spacer layers used in this work exhibit behavior consistent with the presence of significant potential barriers at the collector-base junction resulting from boron out-diffusion [8] from the SiGe base into the Si collector. The impact that potential barriers of this nature can have on neutral base recombination can be quite complex requiring detailed physical modeling [9].

APPENDIX A

The increase in collector current due to avalanche multiplication in a reverse biased collector-base space charge region of a bipolar transistor that is in forward active operation can be modeled by a well known empirical relation [2]

$$I_C = \left(\frac{M\alpha_F}{1 - M\alpha_F}\right) I_{BM}, \quad M = \frac{1}{1 - (V_{cb}/BV_{cbo})^n}. \tag{2}$$

M is the multiplication factor, α_F is the forward common-base current gain, V_{cb} is the reverse collector-base bias, BV_{cbo} is the collector-base breakdown voltage, and I_{BM} is the reverse base current which is generated by the avalanche multiplication process and which opposes the normal forward base current. The parameter n is empirically determined from experimental measurements which usually has a value from 3 to 6 for conventional silicon p-n junctions [2]. Assuming that α_F is close to unity, the reverse base current can be approximated by

$$\begin{aligned} I_{BM} &= I_B(0) - I_B(V_{cb}) \\ &\approx I_C\left(\frac{1-M}{M}\right) = -I_C\left(\frac{V_{cb}}{BV_{cbo}}\right)^n \end{aligned} \tag{3}$$

where I_{BM} has been expressed as the difference between the total base current for zero V_{cb}. $I_B(0)$, and the total base current for a nonzero V_{cb}. $I_B(V_{cb})$, assuming that negligible reverse base current is generated by avalanche breakdown for zero collector-base bias. Rearranging (3) one obtains

$$\left(\frac{I_B(V_{cb}) - I_B(0)}{I_C}\right)^{1/n} = \left(\frac{V_{cb}}{BV_{cbo}}\right). \tag{4}$$

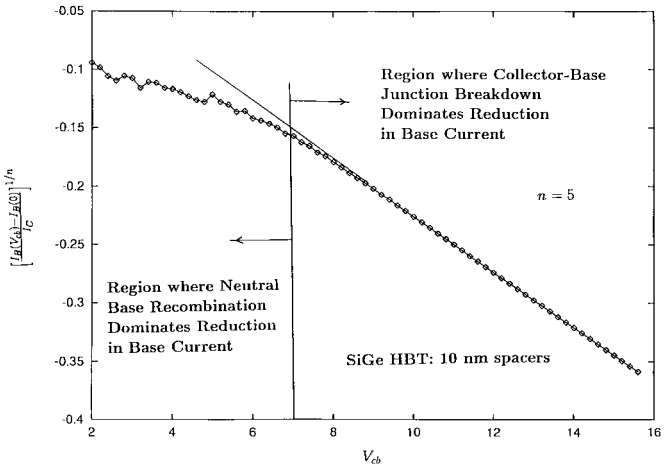

Fig. 3. Experimental measurement of change in base current with increasing reverse collector base bias V_{cb} where data is plotted according to (1) for $n = 5$.

ACKNOWLEDGMENT

The author wishes to thank P. Ashburn of the Microelectronics Group in the Department of Electronics and Computer Science at the University of Southampton, for providing SiGe devices.

REFERENCES

[1] A. Joseph, J. Cressler, R. Jaeger, D. Richey, and D. Harame, "Neutral base recombination in advanced SiGe HBT's and its impact on the temperature characteristics of precision analog circuits," in *IEDM Tech. Dig.*, 1995, pp. 755–756.

[2] P. Gray and R. Meyer, *Analysis and Design of Analog Integrated Circuits*. New York: Wiley, 1993, 3rd ed.

[3] Z. Shafi, C. Gibbings, P. Ashburn, I. Post, C. Tuppen, and D. Godfrey, "The importance of neutral base recombination in compromising the gain of Si/SiGe heterojunction bipolar transistors," *IEEE Trans. Electron Devices*, vol. 38, pp. 1973–1976, Aug. 1991.

[4] J. Hamel, R. Alison, and R. Blaikie, "Experimental method to extract ac collector-base resistance from SiGe HBT's," in *26th Europ. Solid-State Device Research Conf. (ESSDERC)*, 1996, pp. 753–756.
[5] *HP 4155A Semiconductor Parameter Analzer*, Yokogawa-Hewlett Packard, Ltd., 1994.
[6] Z. Shafi, P. Ashburn, I. Post, D. Robbins, W. Leong, C. Gibbings, and S. Nigrin, "Analysis and modeling of the base currents of $Si/Si_{1-x}Ge_x$ heterojunction bipolar transistors fabricated in high and low oxygen content material," *J. Appl. Phys.*, vol. 78, pp. 2823–2829, Aug. 1995.
[7] D. Roulston, *Bipolar Semiconductor Devices*. New York: McGraw-Hill, 1990.
[8] E. Prinz, P. Garone, P. Schwartz, X. Xiao, and J. Sturm, "The effects of base dopant outdiffusion and undoped $Si_{1-x}Ge_x$ junction spacer layers in $Si/Si_{1-x}Ge_x$ heterojunction bipolar transistors," *IEEE Electron Device Lett.*, vol. 12, pp. 42–44, Feb. 1991.
[9] S.-I. Kim, B. Ryum, S.-W. Kang, and W. Kim, "The effect of a parasitic potential barrier on the neutral base current recombination current of Si/SiGe/Si DHBT's," *Solid-State Electron.*, vol. 37, pp. 517–519, Mar. 1994.

Optimum Collector Width of VLSI Bipolar Transistors for Maximum $f_{\max}$ at High Current Densities

M. Jagadesh Kumar and Krishanu Datta

***Abstract*—A simple analytical model for optimum collector epi-layer thickness $W_{\rm epi}$ to maximize $f_{\max}$ of VLSI bipolar transistors having reach-through collector is reported. Numerical and analytical results for $W_{\rm epi}$ are compared to verify the validity of our model for the optimum collector epi-layer thickness at high current densities.**

I. Introduction

The maximum oscillation frequency or unity gain frequency $f_{\max}$ determines the maximum frequency of operation of bipolar junction transistors. Hence $f_{\max}$ is a very important parameter for the design of advanced bipolar junction transistor. Although the high-performance bipolar transistors are increasingly designed to operate at lower power levels, as the device dimensions are scaled down, they are forced to operate at high current densities, approaching Kirk current density, to maintain reasonable operating current levels. However due to the resultant base push out effect, the value of $f_{\max}$ reduces significantly at high current densities [1]. High-performance transistors operating at high current densities are also prone to the avalanche breakdown at the CB junction. To avoid this problem, a reduced field design concept has been suggested and demonstrated [2,3] in which a lightly doped (10^{15}–$10^{16}/\text{cm}^3$) i-layer is formed between the collector-base junction and the highly doped collector. Transistors with this thin reach-through collector structure have higher current carrying capacity and less vertical base stretching and improved breakdown voltage, thus offering better high-frequency performance at high current densities as compared to transistors with highly doped collector structure [4]. Hence, designing the optimum collector thickness $W_{\rm epi}$ of the i-layer to achieve maximum $f_{\max}$ is of interest to device designers. The aim of the present paper is, therefore, to provide a simple analytical model for optimum $W_{\rm epi}$ to maximize $f_{\max}$ at Kirk current density. We have shown the validity of our analytical expression for a realistic polysilicon emitter transistor having reach-through collector structure by comparing the analytical results for $W_{\rm epi}$ with numerical results obtained using BIPOLE3 simulator [5].

Manuscript received July 24, 1996; revised November 8, 1996. The review of this brief was arranged by Editor T. Nakamura.

M. J. Kumar is with the Department of Electrical Engineering, Indian Institute of Technology, Delhi, Hauz Khas, New Delhi 110 016, India.

K. Datta was with IC Design Eng., MPD Group, Texas Instruments (India) Ltd., Bangalore 560 017, India. He is now with Department of Electrical Engineering, Indian Institute of Technology, Delhi, Hauz Khas, New Delhi 110 016, India.

Publisher Item Identifier S 0018-9383(97)03016-5.

II. Theory

For polysilicon emitter transistor, the various vertical delay times are

$$\sum_i t_i = t_{\rm pol} + t_{em} + t_{bb} + t_{qbe} + t_{\rm scl} + \frac{C_{je} + C_{jc}}{g_m} \tag{1}$$

where $t_{\rm pol}$ is the delay due to minority charge transport through poly-layer, t_{em} is the delay due to minority charge in the neutral emitter, t_{bb} is the delay due to minority charge in the neutral base, t_{qbe} is the delay due to free carrier charge in the emitter-base space-charge layer and $t_{\rm scl}$ is the collector-base space-charge layer delay. C_{je} and C_{jc} are the emitter-base and collector-base depletion capacitances. In (1), the time constant R_cC_{jc} is neglected for the simplification of the analysis. In terms of the above delay times, $f_{\max}$ can be written as [6]

$$f_{\max} = \frac{1}{4\pi r_{bb}^{1/2}} \sqrt{\frac{1}{C_{jc}\sum_i t_i}} \tag{2}$$

where r_{bb} is the base resistance, C_{jc} is the collector-base space-charge layer capacitance and $\Sigma_i\ t_i$ is the sum of all vertical delays. The maximum oscillation frequency $f_{\max}$ is an important parameter determining the frequency response of a transistor. To get a simple analytical model for collector epi-layer thickness $W_{\rm epi}$ for which $f_{\max}$ is maximum, the following assumptions have been made:

1) the emitter and base profiles are fixed and the emitter-base and base-collector junctions are one sided and abrupt;
2) base doping profile is near uniform;
3) the collector doping is low enough so that at normal reverse bias voltage of V_{CB} the whole collector is depleted;
4) the emitter and collector contact resistance and the extrinsic component of the base resistance are negligible;
5) emitter current crowding effect and base conductivity modulation are negligible;
6) no velocity overshoot effect;
7) and for a given V_{CB}, the collector current density J_C is equal to the Kirk current density J_K.

The condition to be satisfied to get optimum $W_{\rm epi}$ to maximize $f_{\max}$ is [6]

$$\frac{df_{\max}}{dW_{\rm epi}} = 0. \tag{3}$$

Using (2), the above condition becomes

$$C_{jc}\frac{d}{dW_{\rm epi}}\sum_i t_i + \sum_i t_i \frac{dC_{jc}}{dW_{\rm epi}} = 0 \tag{4}$$

where C_{jc}, the junction capacitance per unit area is given by [6]

$$C_{jc} = \frac{k\epsilon}{W_{\rm scl}} \tag{5}$$

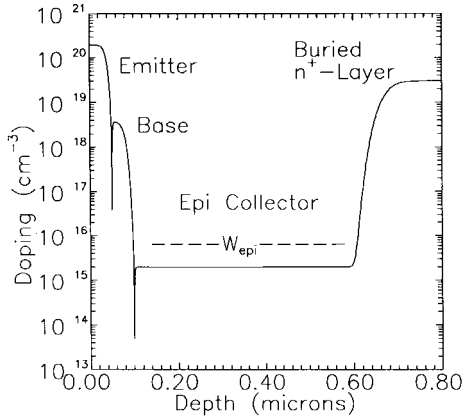

Fig. 1. The doping profile of a single poly high-performance transistor with reach-through collector structure used in BIPOLE3 simulation.

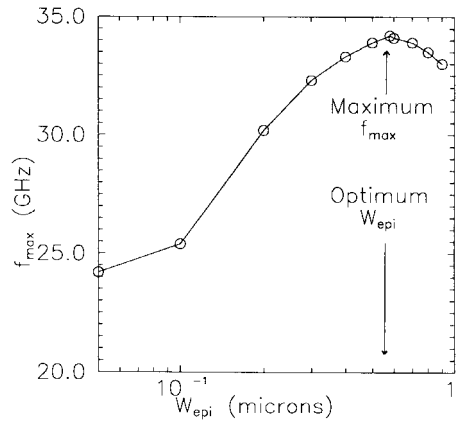

Fig. 2. The maximum frequency of oscillation $f_{\max}$ plotted as a function of the collector epi-thickness $W_{\rm epi}$ at $J_C = J_K$.

where k accounts for the excess charge as $n_c > N_{\rm epi}$ at $J_C = J_K$, n_c is the free electron concentration in collector-base space-charge layer and $W_{\rm scl}$ is the collector space-charge layer width. For reach-through collector structure $W_{\rm scl}$ can be replaced by $W_{\rm epi}$ and taking $k = 1$, (5) can be expressed as

$$C_{jc} = \frac{\epsilon}{W_{\rm epi}}. \tag{6}$$

Differentiating C_{jc} with respect to $W_{\rm epi}$ we get

$$\frac{dC_{jc}}{dW_{\rm epi}} = -\frac{\epsilon}{W_{\rm epi}^2}. \tag{7}$$

Among vertical delays, $\Sigma_i\ t_i, t_{\rm pol}, t_{em}$ and t_{bb} are roughly independent of collector current density for $J_C \le J_K$. The collector space-charge layer delay time can be expressed as [7]

$$t_{\rm scl} = \frac{W_{\rm scl}}{2\upsilon_s} \tag{8}$$

where υ_s is the saturated electron drift velocity. Since we are considering a reach-through collector in our analysis, (8) changes to

$$t_{\rm scl} = \frac{W_{\rm epi}}{2\upsilon_s}. \tag{9}$$

The last term in (1) is given by

$$\frac{C_{je} + C_{jc}}{g_m} = \left[C_{je} + \frac{\epsilon}{W_{\rm epi}}\right]\frac{V_T}{J_C}. \tag{10}$$

The Kirk current density J_K for reach-through collector structure is [4]

$$J_K = 2\epsilon\upsilon_s\frac{V_{CB}}{W_{\rm epi}^2} \tag{11}$$

where V_{CB} is the externally applied reverse bias voltage including the built-in potential. Substituting (11) into (10), we have

$$\begin{aligned}\frac{C_{je} + C_{jc}}{g_m} &= \left[C_{je} + \frac{\epsilon}{W_{\rm epi}}\right]\frac{V_T W_{\rm epi}^2}{2\epsilon\upsilon_s V_{CB}} \\ &= \left[\frac{C_{je}W_{\rm epi}^2}{\epsilon} + W_{\rm epi}\right]\frac{V_T}{2\upsilon_s V_{CB}}.\end{aligned} \tag{12}$$

Hence at $J_C = J_K$ the sum of all vertical delays can be expressed as

$$\begin{aligned}\sum_i t_i =& t_{\rm pol} + t_{em} + t_{bb} + t_{qbe} + \frac{W_{\rm epi}}{2\upsilon_s} \\ &+ \left[\frac{C_{je}W_{\rm epi}^2}{\epsilon} + W_{\rm epi}\right]\frac{V_T}{2\upsilon_s V_{CB}}.\end{aligned} \tag{13}$$

Therefore, using (13), the term $(d/dW_{\rm epi})\ \sum_i\ t_i$ in (4) is given by

$$\frac{d}{W_{\rm epi}}\sum_i t_i = \frac{1}{2\upsilon_s}\left[1 + \frac{V_T}{V_{CB}}\left(1 + \frac{2W_{\rm epi}C_{je}}{\epsilon}\right)\right]. \tag{14}$$

Substituting (6), (7), (13), and (14) in (4) we get

$$\begin{aligned}0 =& \frac{\epsilon}{W_{\rm epi}}\left[\frac{1}{2\upsilon_s}\left[1 + \frac{V_T}{V_{CB}}\left(1 + \frac{2W_{\rm epi}C_{je}}{\epsilon}\right)\right]\right] \\ &- \left[t_{\rm pol} + t_{em} + t_{bb} + t_{qbe} + \frac{W_{\rm epi}}{2\upsilon_s}\right. \\ &\left. + \left(\frac{C_{je}W_{\rm epi}^2}{\epsilon} + W_{\rm epi}\right)\frac{V_T}{2\upsilon_s V_{CB}}\right]\frac{\epsilon}{W_{\rm epi}^2}.\end{aligned} \tag{15}$$

After simplification, the optimum collector epi-thickness $W_{\rm epi}$ can be written as

$$W_{\rm epi} = \sqrt{\frac{t_{\rm pol} + t_{em} + t_{bb} + t_{qbe}}{C_{je}V_T/2\epsilon\upsilon_s V_{CB}}}. \tag{16}$$

Considering emitter-base junction to be abrupt and one sided C_{je} at Kirk current density can be expressed as [1]

$$C_{je} = \frac{\epsilon}{W} = \frac{\epsilon}{\sqrt{\frac{2\epsilon}{qN_B}(V_{bi} - V_{BE})}} \tag{17}$$

where W is the emitter-base space-charge layer width, V_{bi} is the emitter-base built in potential, N_B is the base doping concentration, V_{BE} is the applied forward bias voltage. At high current density where n_c is more than $N_{\rm epi}$, high injection effects become significant [Webster effect] and the base delay t_{bb} can be expressed as [8]

$$t_{bb} = \frac{W_B^2}{4D_n} + \frac{W_B}{\upsilon_s} \tag{18}$$

where W_B is the neutral base width and D_n is the average electron drift velocity in base region. Considering the doping profile of a typical poly-silicon emitter advanced bipolar transistor, as discussed in the following section, BIPOLE3 [5] simulation results show that near Kirk current density J_K, the delays $t_{em}, t_{bb}, t_{\rm pol}$, and t_{qbe} are approximately equal. Hence, as a rough approximation, we can assume that

$$t_{\rm pol} + t_{em} + t_{bb} + t_{qbe} \approx 4t_{bb} = 4\left(\frac{W_B^2}{4D_n} + \frac{W_B}{\upsilon_s}\right). \tag{19}$$

Substituting (17), (18), and (19) in (16) we get

$$W_{\rm epi} = \sqrt{\frac{8\upsilon_s}{V_T}\sqrt{\frac{2\epsilon}{q}}\left(\frac{W_B^2}{4D_n} + \frac{W_B}{\upsilon_s}\right)\left[\frac{V_{bi} - V_{BE}}{N_B}\right]^{1/2}V_{CB}} \tag{20}$$

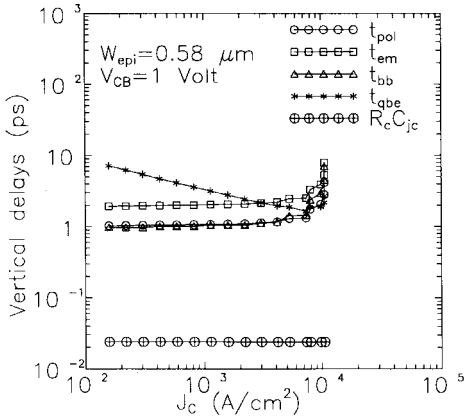

Fig. 3. All vertical delays plotted as a function of collector current density for $W_{\rm epi} = 0.58$ μm at $V_{CB} = 1$ V.

Considering $v_s = 10^7$ cm/s, $V_T = 0.0259$ V $W_{\rm epi}$ can be simplified as

$$W_{\rm epi} = 3.33 \times 10^6 \sqrt{\left(\frac{W_B^2}{4D_n} + \frac{W_B}{v_s}\right)\left[\frac{V_{bi} - V_{BE}}{N_B}\right]^{1/2} V_{CB}} \quad (21)$$

To find optimum $W_{\rm epi}$ from (21), we need to know only the measurable parameters of the transistor e.g., base width W_B, emitter doping N_E, base doping N_B, and the applied voltages across both the junctions. Hence, if the above parameters are known, (21) can predict the value of optimum $W_{\rm epi}$ for a given V_{CB} for which the unity gain frequency $f_{\rm max}$ is maximized at Kirk current density.

III. Simulation and Discussion

To verify the validity of our simple analytical model for optimum $W_{\rm epi}$, we have performed numerical simulations using BIPOLE3 [5] simulator. We have considered a typical single poly high-performance transistor as shown in Fig. 1. The junction depths and device dimensions are similar to those found in realistic devices reported in the literature [9]. We have given the following input parameters to BIPOLE3 simulator: emitter stripe length is 20 μm, emitter stripe width is 0.54 μm, emitter-base junction depth x_{je} is 0.05 μm, base-collector junction depth x_{jb} is 0.1 μm, poly thickness is 0.2 μm, poly layer doping concentration is $10^{20}/\text{cm}^3$, peak base doping is $3.8 \times 10^{18}/\text{cm}^3$, and collector epi-layer doping concentration is $2 \times 10^{15}/\text{cm}^3$. The base is chosen to be near uniformly doped as shown in Fig. 1. Simulation results show that the peak gain of the transistor is approximately 100. Using BIPOLE3, we have first estimated the peak value of $f_{\rm max}$ (corresponding to the Kirk current density) for a given value of $W_{\rm epi}$. We have then plotted this peak $f_{\rm max}$ as a function of $W_{\rm epi}$ in Fig. 2. The values of $W_{\rm epi}$ are varied from 0.05 μm to 1.0 μm. We note that the value of $f_{\rm max}$ becomes maximum for collector epi-layer thickness $W_{\rm epi}$ within 0.5–0.6 μm for $V_{CB} = 1$ V. Substituting $W_B = 0.05$ μm, $N_B = 3.8 \times 10^{18}/\text{cm}^3$, $v_s = 10^7$ cm/s, $V_{CB} = 1$ V, $V_{bi} - V_{BE} \approx 0.075$ V and $D_n \approx 4$ cm^2/s [10] in our final analytical (21) for optimum $W_{\rm epi}$, we obtain $W_{\rm epi}$ to be 0.567 μm. This value is very close to that obtained using BIPOLE3 simulator. Although we have verified (21) for different V_{CB} values, we have given our results for $V_{CB} = 1$ V, since this will be of interest in low voltage applications. The value of $V_{bi} - V_{BE} \approx 0.075$ V at Kirk current density is reasonable as we have verified using BIPOLE3 simulator. Earlier in our analysis we assumed that t_{em}, t_{qbe}, t_{bb}, and $t_{\rm pol}$ are equal. This assumption is verified in Fig. 3 where different delays are plotted as a function of collector current density for $W_{\rm epi} = 0.58$ μm at $V_{CB} = 1$ V. The delay times are obtained using BIPOLE3 simulator. In this figure the value of $t_{\rm pol}, t_{em}, t_{bb}$, and t_{qbe} are approximately equal at Kirk current density and the value of t_{bb} is 2.05 ps. Equation (18) gives the value of t_{bb} to be 2 ps. Thus our analytical model (21) for $W_{\rm epi}$ needs only physical parameters of the device and the operating voltages, for estimating optimum $W_{\rm epi}$ to maximize $f_{\rm max}$ at high current density.

IV. Conclusions

In conclusion, we have developed an analytical model for optimum collector layer thickness $W_{\rm epi}$ to get maximum $f_{\rm max}$ at Kirk current density. By comparing the value of $W_{\rm epi}$ obtained from our analytical model with that obtained using numerical simulation, we have demonstrated the accuracy of our model for predicting optimum $W_{\rm epi}$.

References

[1] D. J. Roulston, *Bipolar Semiconductor Devices*. New York: McGraw-Hill, 1990.
[2] D. D. Tang and P. Lu, *IEEE Electron Device Lett.*, vol. 10, pp. 67–69, 1989.
[3] P. Lu, J. H. Comfort, D. D. Tang, B. S. Meyerson, and J. Y.-C. Sun, *IEEE Electron Device Lett.*, vol. 11, pp. 336–339, 1990.
[4] M. J. Kumar, A. D. Sadovnikov, and D. J. Roulston, *IEEE Trans. Electron Devices*, vol. 40, pp. 1478–1483, 1993.
[5] D. J. Roulston, *NASCODE VII Proc.* Boulder, CO: Front Range Press, 1991, pp. 108–110.
[6] M. J. Kumar and D. J. Roulston, *Solid-State Electron.*, vol. 37, pp. 1885–1887, 1994.
[7] J. M. Early, *Bell Syst. Technol.*, vol. 33, p. 517, 1954.
[8] J. J. H. van Den Biesen, *Solid-State Electron.*, vol. 29, pp. 529–534, 1986.
[9] P. V. Voorde, D. Pettengill, and S.-Y. Oh, in *Proc. BCTM*, 1990, pp. 114–117.
[10] W. E. Beadle, J. C. C. Tsai, and R. D. Plummer, *Quick Reference Manual For Silicon Integrated Circuit Technology*. New York: Wiley, 1985.

An Improved Small-Signal Equivalent Circuit Model for III–V Nitride MODFET's with Large Contact Resistances

Jinwook Burm, William J. Schaff, Lester F. Eastman, Hiroshi Amano, and Isamu Akasaki

***Abstract*— A small-signal equivalent circuit model of III–V nitride MODFET's is presented. The metal-semiconductor ohmic contacts were modeled as a transmission line, as parasitic Z-elements cannot be modeled as a simple resistor/inductor discrete circuit due to high contact resistances. The model describes the highly resistive contacts with a good accuracy.**

The potential of III–V nitride materials for device applications has been widely recognized with the successful demonstration of blue lasers [1], [2] as well as highly efficient light emitting diodes [3]. In addition to the successes in optical devices, GaN based FET's (Field Effect Transistors) have demonstrated excellent high frequency performances showing cut-off frequency (f_T) of 36.1 GHz [4] and maximum oscillation frequency $(f_{\max})$ of 77 GHz [5]. However, newly developed III–V nitride FET's still suffer from high source and drain resistances due to immature processing technology. Typical values of source resistance vary from 7 to 30 Ω/mm [4]–[6]. To examine the intrinsic properties for GaN based FET's, it is necessary to extract parasitics associated with the pad capacitances and access impedances. However due to the presently high contact resistances, the standard circuit model extraction method [7]–[10] cannot be performed in ordinary ways and a special method is required to extract the Z-parasitic elements. A different circuit model extraction method for III–V nitride FET's will be discussed in this paper, the results of which can be applied to general FET's with high contact resistances. The circuit model presented in this paper is performed for a MODFET (Modulation Doped Field Effect Transistor) on a III–V nitride [5] with a gate width of 100 μm and a 2-μm source-drain spacing. The gate length of the device was 0.25 μm. The OMVPE grown MODFET layers included, from the bottom, a (0001) Sapphire substrate, low temperature grown AlN buffer, 3–5-μm thick GaN, 200 Å $Al_{0.16}Ga_{0.84}N$ charge confining layer, 75 Å GaN channel, 50 Å $Al_{0.16}Ga_{0.84}N$ spacer, 20 Å Si doped $Al_{0.16}Ga_{0.84}N$, 130 Å $Al_{0.16}Ga_{0.84}N$ barrier, and 60 Å Si-doped $Al_{0.06}Ga_{0.94}N$ cap layer. Si doping density was 2×10^{18} cm^{-3}. The MODFET's were fabricated through ohmic metal, proton-implanted isolation, and gate metal processes. The ohmic metal was Ni/AuSi/Ag/Au (100 Å/1000 Å/1000 Å/1500 Å) annealed at 750 °C for 30 s under N_2 atmosphere. The dc contact resistance of the ohmic contacts was 9.2 Ω/mm. The gate metal was Ti/Pd/Au [5]. For S-parameter measurements, an HP8510B network analyzer was utilized in the frequency range from 45 MHz to 26.5 GHz.

The contributions from parasitic capacitances between pads (open Y-parasitics) were determined from separate test patterns [7], [9]. The separate open test patterns for the parasitic capacitances had the identical lay-out with the regular FET's and were fabricated on an isolated part of the wafer. From the standard methods [8], [9] with the S-parameters of the open test patterns, parasitic capacitance values were determined to be 10.3 fF for parasitic gate-source capacitance (C_{pgs}), 2.76 fF for parasitic gate-drain capacitance (C_{pgd}), and 20.8 fF for parasitic drain-source capacitance (C_{pds}).

Parasitic resistances and inductances (Z-parasitics) of drains and sources can be deduced from the S-parameters by forcing large gate currents with zero drain-source bias, the short bias condition [8]. Under this short bias condition, the source and drain contacts are normally represented with a resistor and an inductor in series. However for highly resistive contacts the capacitive nature of metal-semiconductor ohmic contact, which is often negligible for a good ohmic contact, becomes important. As a result, the measured S_{11} and S_{22}, even with an excessive positive gate bias, look capacitive rather than showing the usual inductive characteristics (not shown), making the determination of parasitic resistances and inductances impossible.

To solve this problem the sources and drains were modeled with transmission lines for the metal-semiconductor contacts, resistors for the resistance in the semiconductor $(R_{\rm in})$ and in the metal (R_p), and an inductor for the metal pad (L_p) (Fig. 1 inset). The transmission lines are represented with the resistance per unit length along the current path (along the contacts) (R), the shunt conductance per unit length (G), and the capacitance per unit length (C). The L_p's and R_p's of metal contacts were determined from short test patterns fabricated with source and drain pads connected with metal over the mesa area. In addition to the L_p's and R_p's from the metal pads, the contributions from parasitic capacitances between the pads were stripped from the measured S-parameters at a short bias condition. Following the analysis as described in [11], the source or drain resistance after stripping the parasitics from metal pads is

$$R_{\rm in} + \sqrt{\frac{R}{G+j\omega C}}\coth\left(\frac{d}{L_t}\right) \approx R_{\rm in} + \sqrt{\frac{R}{(G+j\omega C)}} = R_{\rm in} + \sqrt{\frac{1}{(x+j\omega y)}} \quad (1)$$

where d is the overlap between the metal and semiconductor in the direction of current path, L_t is the transfer length of the contact, x is G/R, and y is C/R. The coth term is nearly equal to 1 as L_t was measured to be 5.4 μm and d was 20 μm. From the measured S-parameters of the actual MODFET's with excessive positive gate bias for the gate current of 100 mA/mm and a dc measurement [$\omega = 0$ in (1)], $R_{\rm in}$ was 21.85 Ω, x was 6.1×10^{-5} Ω^{-2}, and y was 1.3×10^{-14} F/Ω for the source of the 100-μm wide device. From the Hall measurement of the wafer, R was 12 600 Ω/mm, and consequently G is 760 mS/mm and C is 163 pF/mm. The calculated results from the solutions are compared with the measured result for the source contact (Fig. 1), showing a good agreement. The same analysis was done for the drain, and the result was almost identical to that of the source. The capacitive nature of ohmic contacts is also critical at ultra-high frequencies (~100 GHz). Tasker *et al.* [10] have used a second set of parasitic capacitors for the modeling at this frequency region.

Manuscript received April 18, 1996; revised November 23, 1996. The review of this brief was arranged by Editor P. M. Solomon. The work at Cornell University was supported by the Office of Naval Research under Contract N00014-95-1-0926. The work at Meijo University was supported in part by the Ministry of Education, Science, Sports, and Culture of Japan (High-Tech Research Center, under Contracts 06452114, 07505012, and 07650025), Japan Society of the Promotion of Science (Research for the Future), and Daiko Foundation.

J. Burm, W. J. Schaff, and L. F. Eastman are with the School of Electrical Engineering and Cornell Nanofabrication Facility, Cornell University, Ithaca, NY 14853 USA.

H. Amano and I. Akasaki are with the Department of Electrical and Electronic Engineering, Meijo University, Nagoya, Japan.

Publisher Item Identifier S 0018-9383(97)03017-7.

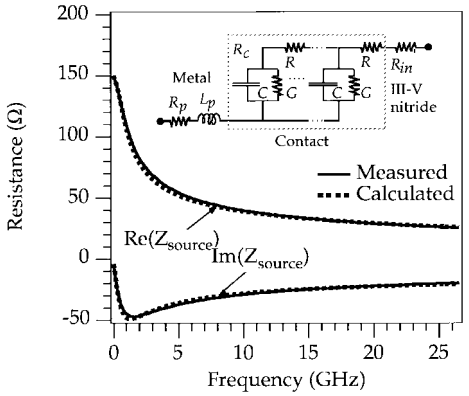

Fig. 1. Measured and calculated source impedance $Z_{\rm source}$ at a short biased condition as a function of frequency. The inset is the reactance model of sources and drains. R_p was 0.045 Ω/mm, L_p was 10 pH, R was 12600 Ω/mm, G was 760 mS/mm, and C was 163 pF/mm for the source.

The intrinsic elements of MODFET's were determined after the extraction of the Y and Z-parasitic elements [7]–[9]. The calculated S-parameters based on the intrinsic elements agreed well with the measured values (not shown). The extrinsic f_T and $f_{\rm max}$ determined from the measured S-parameters were 16.3 GHz and 50.7 GHz, respectively, at the gate bias of -1 V and the drain bias of 20 V. From the determined intrinsic equivalent circuit elements the intrinsic f_T is 21 GHz, a 29% increase compared with the extrinsic f_T of 16.3 GHz.

In conclusion, a small-signal equivalent circuit model for III–V nitride MODFET's was determined through parasitic extractions. Due to the high contact resistance of current III–V nitride MODFET's, a special method was required to extract the Z-parasitic elements. The highly resistive source and drain contacts were modeled as transmission lines and each element in the transmission line was determined from the Z-parasitic measurements. After the parasitic stripping, the intrinsic elements were determined using the standard method [7]–[9]. The calculated elements were checked by calculating the S-parameters of the equivalent circuit and comparing these with the measured S-parameters, which exhibited good agreements. In addition to the III–V nitride transistors, this method can be applied to transistors with high contact resistances, such as transistors on SiC based materials and future material systems.

ACKNOWLEDGMENT

The authors wish to thank G. H. Martin and K. Chu for helpful discussions.

REFERENCES

[1] S. Nakamura, M. Senoh, S-i Nagahama, N. Iwasa, T. Yamada, T. Matsushita, H. Kiyoku, and Y. Sugimoto, "InGaN-based multi-quantum-well-structure laser diodes," *Jpn. J. Appl. Phys.*, vol. 35, pp. L74–L76, 1996.

[2] I. Akasaki, S. Sota, H. Sakai, T. Tanaka, M. Koike, and H. Amano, "Shortest wavelength semiconductor laser diode", *Electron. Lett.*, vol. 32, pp. 1105–1106, 1996.

[3] S. Nakamura, M. Senoh, N. Iwasa, and S.-i. Nagahama, "High-power InGaN single-quantum-well-structure blue and violet light-emitting diodes," *Appl. Phys. Lett.*, vol. 67, pp. 1868–1870, 1995.

[4] M. A. Khan, Q. Chen, M. S. Shur, B. T. Dermott, J. A. Higgins, J. Burm, W. Schaff, and L. F. Eastman, "Short-channel GaN/AlGaN doped channel heterostructure field effect transistors with 36.1 cutoff frequency," *Electron. Lett.*, vol. 32, pp. 357–358, 1996.

[5] J. Burm, W. J. Schaff, and L. F. Eastman, H. Amano, and I. Akasaki, "75 Å GaN channel modulation doped field effect transistors," *Appl. Phys. Lett.*, vol. 68, pp. 2849–2851 (1996).

[6] M. A. Khan, J. N. Kuznia, D. T. Olson, W. J. Schaff, J. Burm, and M. S. Shur, "Microwave performance of a 0.25-μm gate AlGaN/GaN heterostructure field effect transistor," *Appl. Phys. Lett.*, vol. 65, pp. 1121–1123, 1994.

[7] B. Hughes and P. J. Tasker, "Bias dependence of the MODFET intrinsic model elements values at microwave frequencies," *IEEE Trans. Electron Devices*, vol. 36, pp. 2267–2273, 1989.

[8] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the FET small-signal equivalent circuit," *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 1151–1159, 1988.

[9] M. Berroth and R. Bosch, "High-frequency equivalent circuit of GaAs FET's for large-signal applications," IEEE *Trans. Microwave Theory Tech.*, vol. 39, pp. 224–229, 1991.

[10] P. J. Tasker and J. Braunstein, "New MODFET small-signal circuit model required for millimeterwave MMIC design: Extraction and validation to 120 GHz," in *Proc. 1995 IEEE MTT-S Dig.*, Orlando, FL, 1995, pp. 611–614.

[11] R. Williams, *Modern GaAs Processing Methods*. Norwood, MA: Artech House, 1990, pp. 211–239.

Planar 6H-SiC MESFET's with Vanadium Implanted Channel Termination

Man Pio Lam, Kevin T. Kornegay, James A. Cooper, Jr., and Michael R. Melloch

***Abstract*—We use vanadium ion implantation to form a highly resistive surface layer in the wide bandgap semiconductor silicon carbide (SiC). MESFET's are successfully fabricated using this highly resistive layer to isolate gate metal extensions along the channel width from the p-type epilayer. Fabrication and characterization of these devices are described in this paper.**

In recent years, significant progress in crystal growth and epitaxy of 6H-SiC has led to increased attention to this excellent wide bandgap semiconductor (3.0 eV for the 6H polytype). Its high breakdown electric field ($\sim$10 $\times$ that of silicon) and high electron saturation drift velocity (2×10^7 cm/s) make the realization of high-power and high-frequency devices feasible. SiC MOSFET's and MESFET's have been fabricated in integrated form, such as monolithic NMOS digital IC's [1], MOS analog IC's [2], CMOS IC's [3], and Schottky diode FET inverters [4]. Since MOS devices suffer oxide degradation at a temperature above 300 °C, JFET's and MESFET's are more suitable for high-temperature electronics.

SiC crystals with semi-insulating behavior have been grown with doped vanadium using the physical vapor transport process [5]. Submicron SiC MESFET's have been fabricated on high resistivity substrates and demonstrate good RF performance [6]. However, conventional mesaisolated structures used in these devices make it

Manuscript received August 7, 1996; revised December 4, 1996. The review of this brief was arranged by Editor K. M. Lau. This work is supported by NSF under Grant 952 190-ECS and ONR/MURI under Grant N00014-95-1-1302.

M. P. Lam, K. T. Kornegay, J. A. Cooper, Jr., and M. R. Melloch are with the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907-1285 USA.

Publisher Item Identifier S 0018-9383(97)03018-9.

difficult to achieve high-density integration. In the case of high-voltage Schottky barrier diodes, argon implantation has been used as edge termination to obtain a nearly ideal breakdown voltage [7]. In addition to edge termination for Schottky diodes, high resistivity regions in selected areas on the wafer can also be used to isolate gate metal extensions along channel widths of MESFET's [8]. This approach is desirable for planar high-density MESFET digital integrated circuits [9]. In this paper, we report the characteristic of a Schottky contact on a highly resistive layer in p-type 6H-SiC produced by vanadium ion implan- tation. The current-voltage ($I-V$) characteristics of a MESFET with vanadium ion implant isolation are experimentally investigated and compared with a MESFET without implant isolation.

Fabrication of MESFET's as shown in Fig. 1 is carried out on a p-type 6H-SiC epilayer doped with Al at 5×10^{15} cm^{-3}. The N^+ source/drain and N^- channel regions are selectively implanted with nitrogen at 650 °C through a Ti/Au implant mask and a 20-nm SiO_2 screen layer. Vanadium is also selectively implanted at 650 °C to isolate metal interconnections from the epilayer. A double energy of 85 keV and 190 keV is used with a total dose of $1.9 \times 10^{14}|$; cm^{-2} for vanadium implantation. A SIMS analysis indicated that a roughly flat concentration of implanted vanadium throughout 0.12 μm and a broad implant tail. All implant species are annealed in a Lindbergh tube furnace in argon at 1200 °C for 12 min. The anneal condition is optimized for N^+ implant [10], yielding a sheet resistance of 1.1 kΩ per square. An Al ohmic contact is fabricated on the backside of the substrate by thermal evaporation and subsequently annealed in argon at 1000 °C for 5 min. Ni is evaporated and patterned by lift-off on the same mask level to form ohmic contacts, Schottky barrier contacts, and interconnections. Before Ni deposition, the epilayer surface is cleaned in organic solvents, BHF, and rinsed in deionized water. Non-alloyed Ni is known to have good Schottky and ohmic behavior on lightly-doped and heavily-doped N-type regions, respectively [10]. CV measurements on N-channel Schottky diodes indicate that the channel doping is about 1.3×10^{17} cm^{-3} and the channel depth is about 140 nm.

Another sample cut from the same wafer is blanket implanted with vanadium ions with a 5.7×10^{12} cm^{-2} dose at 85 keV and 1.3×10^{13} cm^{-2} at 190 keV. The implantation was done at 650 °C through a 20-nm SiO_2 screen layer. Post-implantation annealing was performed with the same condition as the MESFET sample. Au Schottky contacts with an area of 1×10^{-4} cm^{-2} are evaporated and patterned on the clean surface to investigate the conductivity through a vertical Au/V-implanted layer/p-type SiC Schottky barrier diodes. Forward $I-V$ measurements of Au/V-implanted SiC and Au/SiC Schottky diodes at room temperature are shown in Fig. 2. The implanted sample, after annealing at 1200 °C, produces orders of magnitude higher resistivity in comparison with the nonimplanted sample. Further experiments regarding implant dose and anneal conditions are required in order to obtain the optimal highly resistive layer. At 10 V, V-implanted SiC Schottky diodes exhibit specific differential contact resistances up to 3×10^7 ohm-cm^2 and current densities as low as 2×10^{-8} A/cm^2, which is six orders of magnitude less than their unimplanted counterparts. In [11], it was shown that the resistivity of V-implanted p-type 6H-SiC is $10^{12} \sim 10^{13}$ Ω-cm with a 3.0×10^{12} cm^{-2} dose at 400 keV and 2.1×10^{12} cm^{-2} at 300 keV. The resistivity increases only slightly ($2 \times 10^{12} \sim 4 \times 10^{13}$ Ω-cm) when annealed at 1500 °C as compared to $10^{12} \sim 3 \times 10^{13}$ Ω-cm obtained at 1200 °C.

Vanadium atoms are reported to have three possible charge states in 6H-SiC: positive ($3d^0$), neutral ($3d^1$) and negative ($3d^2$). Vanadium acts as a donor ($0/+$) in p-type SiC and an acceptor ($0/-$) in n-type SiC. The position of the donor level in the bandgap of 6H-SiC has been determined to be $\sim E_v + 1.6$ eV [12], [13]. The temperature dependence of the forward current of V-implanted Schottky diode is used to estimate the energy level of vanadium in SiC. Fig. 3 shows current as a function of temperature at a constant forward bias voltage of 0.4 V. A linear fit of the currents measured from three diodes yields an activation energy between 1.31 to 1.41 eV, which is close to the energy levels reported for vanadium in p-type SiC. The current-voltage characteristics of the high resistivity layer demonstrates two regimes. At low voltage, deep level donor states trap the injected carriers and control the resistivity. With increasing bias, the current will rise rapidly due to a complete filling of hole traps. Moreover, the trap barrier height will be reduced by field enhancement at high voltage and consequently, the forward current increases with a lower activation energy.

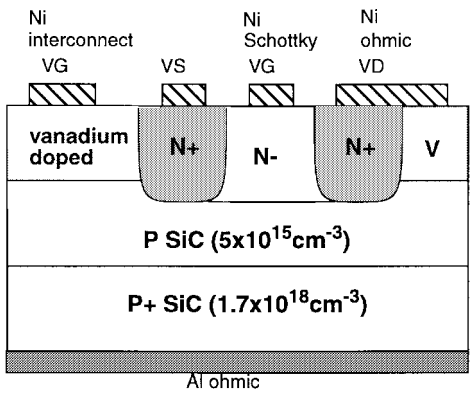

Fig. 1. Cross section of an ion implanted 6H-SiC MESFET along (a) the channel length and (b) the channel width.

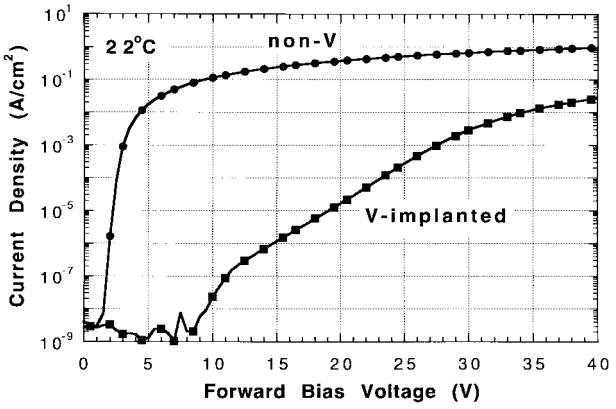

Fig. 2. Forward $I-V$ characteristics of Au/V-implanted SiC and Au/SiC diodes at room temper- ature. Area $= 100 \times 100$ μm.

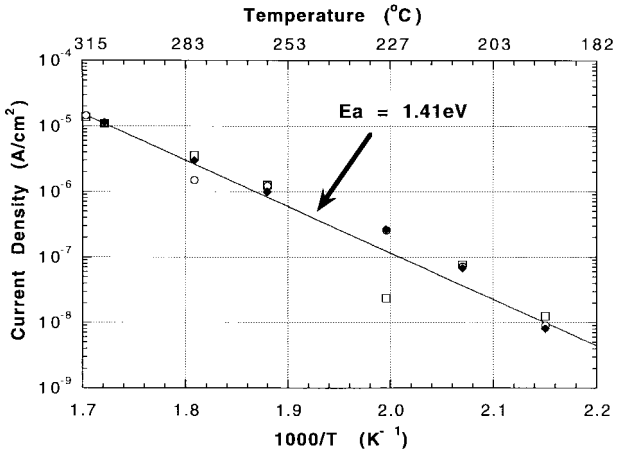

Fig. 3. Current as a function of temperature for three Au/V-implanted 6H-SiC Schottky barrier diodes at a bias of 0.4 V. Activation energy of current is between 1.31 to 1.41 eV.

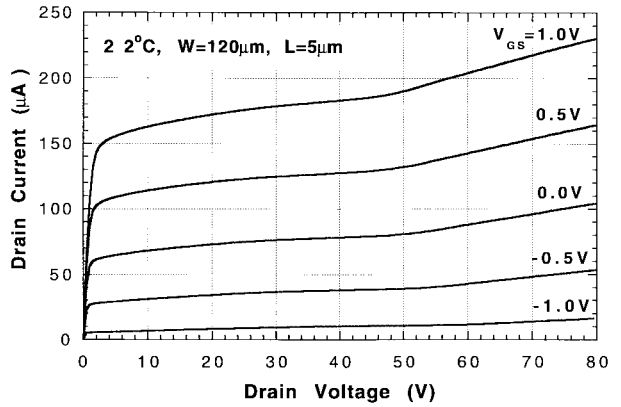

Fig. 4. Output characteristic of a linear MESFET with vanadium isolation at room temperature.

A set of linear MESFET's with different channel lengths and widths are fabricated with vanadium isolation around the channel. The output characteristics of a MESFET with a $W/L = 120\ \mu\text{m}/5\ \mu\text{m}$ is depicted in Fig. 4. The I_{DS} versus V_{GS} plot with $V_{DS} = 50$ mV shown in Fig. 5 indicates a pinch-off voltage $V_p = -1.35$ V, a built-in voltage $V_{bi} = 1.0$ V, and an extrinsic transconductance $g_m = 37\ \mu$S/mm in the linear region at room temperature. The extracted channel mobility is approximately 55 cm^2/V-s at room temperature. The channel mobility of conventional trench isolated JFET's and MESFET's built on n-type epitaxial layer is reported to be close to the SiC bulk mobility (200 cm^2/V-s). Lattice scattering, which originates from the damage by channel implantation, causes the MESFET channel mobility to degrade. At 310 °C, the drain current decreases due to electron mobility degradation at high temperature. V_p shifts by -0.2 V over a temperature range of 22 °C to 310 °C, and g_m is 15 μS/mm at 310 °C.

Since the Schottky gate and interconnection metals overlap the p-type epilayer, on the region without vanadium implant isolation, the Schottky barrier becomes forward biased whenever a negative voltage is applied to the gate. The gate area over the epilayer outside the channel is $80 \times 80\ \mu$m in these devices. Fig. 6 shows the gate, drain and substrate currents of a MESFET without vanadium implant isolation. When the metal gate is positively biased, the gate current flows to the source and drain through the n-channel; with a negative bias, gate current conducts through the substrate. The low

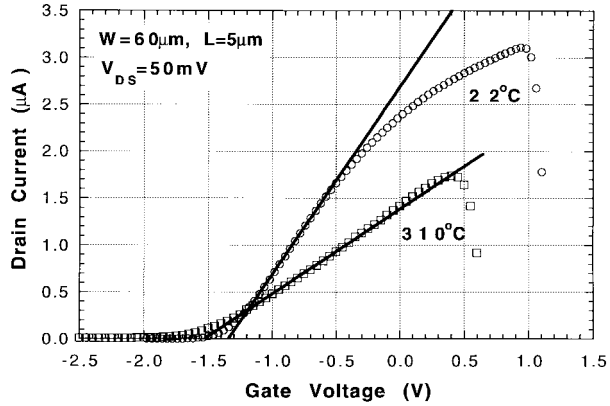

Fig. 5. Linear region characteristic of a 5- μm MESFET with vanadium implant isolation at room temperature and 310 3°C. Maximum transconductance at room temperature is 37 μS/mm.

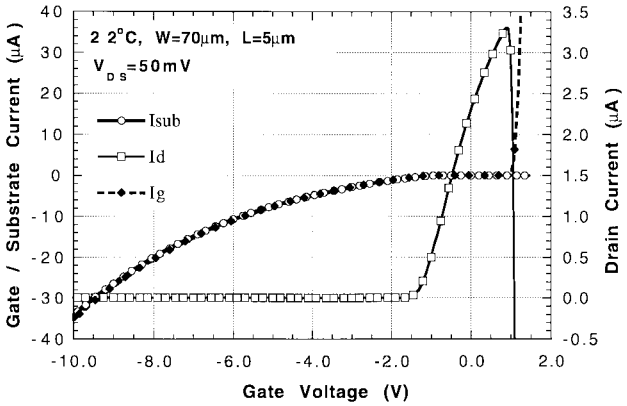

Fig. 6. Drain, gate and substrate current of a MESFET without vanadium implant isolation. Gate area overlap over the p-epilayer is $80 \times 80\ \mu$m.

gate to substrate current in this sample is dominated by the backside contact resistance. The gate to substrate current of its counterpart with vanadium implant isolation is less than 30 nA at a gate voltage of -10 V. The resistivity of V-implanted layer decreases with temperature due to the emission of carriers from the trap. The gate to substrate current is about 15 nA at -3 V gate voltage for the V-implanted MESFET at 310°C.

In conclusion, we have experimentally demonstrated that a highly resistive surface layer can be selectively created in 6H-SiC by vanadium ion implantation. This layer has been used to terminate the gate metal extension along the channel width of the MESFET. For a MESFET with a pinch-off voltage of only several negative volts (higher than -10 V as shown in our case), the gate to substrate leakage current would be blocked by the V-implanted layer. This gate terminated MESFET is suitable for applications in integrated form.

ACKNOWLEDGMENT

The authors would like to thank S.A. Schwarz for SIMS analysis.

REFERENCES

[1] W. Xie, J. A. Cooper, Jr., and M. R. Melloch, "Monolithic NMOS digital integrated circuits in 6H-SiC," *IEEE Electron Device Lett.*, vol. 15, pp. 455–457, Nov. 1994.

[2] D. M. Brown, M. Ghezzo, J. Kretchmer, V. Krishnamurthy, G. Michon, and G. Gati, "High-temperature silicon carbide planar IC technology and first monolithic SiC operational amplifier IC," in *Trans. 2nd High-*

Temperature Electron. Conf., vol. 1, D. B. King and F. V. Thome, Eds., Charlotte, NC, June 5–10, 1994.
[3] D. B. Slater, Jr., G. M. Johnson, L. A. Lipkin, A. V. Suvorov, and J. W. Palmour, "Demonstration of a 6H-SiC CMOS Technology," in *IEEE Device Research Conf.*, Santa Barbara, CA, June 24–26, 1996, pp. 162–163.
[4] G. L. Harris, K. Wongchotigul, H. Henry, K. Diogu, C. Taylor, and M. G. Spencer, "Beta SiC Schottky diode FET inverters grown on silicon," *Inst. Phys. Conf. Ser.*, no. 137, pp. 715–717, 1994.
[5] H. McD. Hobgood, R. C. Glass, G. Augustine, R. H. Hopkins, J. Jenny, M. Skowronski, W. C. Mitchel, and M. Roth, "Semi-insulating 6H-SiC grown by physical vapor transport," *Appl. Phys. Lett.*, vol. 66, no. 11, pp. 1364–1366, Mar. 1995.
[6] S. Sriram, R. C. Clarke, A. A. Burk, Jr., H. M. Hobgood, P. G. McMullin, P. A. Orphanos, R. R. Siergiej, T. J. Smith, C. D. Brandt, M. C. Driver, and R. H. Hopkins, "RF performance of SiC MESFET's on high resistivity substrates," *IEEE Electron Device Lett.*, vol. 15, pp. 458–459, Nov. 1994.
[7] D. Alok, B. J. Baliga, and P. K. McLarty, "A simple edge termination for silicon carbide devices with nearly ideal breakdown voltage," *IEEE Electron Devices Lett.*, vol. 15, pp. 394–395, Oct. 1994.
[8] M. P. Lam, K. T. Kornegay, and J. A. Cooper, Jr., "A highly resistively layer in 6h-sic obtained by vanadium ion implantation," in *Proc. Int. Semiconductor Device Research Symp.*, 1995, pp. 517–519.
[9] M. P. Lam, K. T. Kornegay, J. A. Cooper, Jr., and M. R. Melloch, "Ion implant technology for 6H-SiC MESFET's digital IC's," in *IEEE Device Research Conf.*, Santa Barbara, CA, June 24–26, 1996, pp. 158–159.
[10] N.-H. Pan, "Development of POLYSILICON-GATE MOSFET's in 6H silicon carbide," Ph.D. dissertation, Purdue University, West Lafayette, IN, 1996.
[11] T. Kimoto T. Nakajima, H. Matsunami, T. Nakata, and M. Inoue, "Formation of Semi-Insulating 6H-SiC layers by vanadium ion implantations," *Appl. Phys. Lett.*, vol. 69, pp. 1113–1115, 1996.
[12] J. R. Jenny, M. Skowronski, W. C. Mitchel, H. M. Hobgood, R. C. Glass, G. Augustine, and R. H. Hopkins, "On the compensation mechanism in high-resistivity 6H-SiC-doped with vanadium," *J. Appl. Lett.*, vol. 78, pp. 3839–3842, 1995.
[13] J. Schneider and K. Maier, "Point defects in silicon carbide," *Physica B*, vol. 105, pp. 199–206, 1993.

CMOS-Circuit Degradation Analysis Using Optical Measurement of the Substrate Current

Giovanni Romano and Marco Sampietro

***Abstract*—This paper analyzes the photon emission under ac operation caused by hot carriers in MOSFET's, and determines the lifetime of CMOS circuits by means of a direct photon count measurement that replaces the traditional electrical measurement of the substrate current. This is made possible by the linear relation between the substrate current and the photon count at about 830 nm for all operating values of Gate voltage. The paper presents an application of this method to monitor the long term degradation of the delay time of CMOS inverters and highlights the advantages of this noninvasive technique which can therefore be used to predict the lifetime also of devices in which the substrate current can not be measured directly, as in SOI devices.**

I. Introduction

MOS devices degradation due to hot carriers is extensively studied because of its implications in the scaling of channel length to submicron dimensions. Most of the models developed for the evaluation of n-MOSFET lifetime are based on the experimental measurement of the substrate current $(I_{\rm sub})$ as an index of the hot-carrier population in the device [1], [2]. Only in recent years degradation monitoring by visible light emission from hot carriers has been proposed [3]–[6].

In this paper we introduce a method for MOSFET lifetime prediction based on the measurement of the radiation emitted by the device. The method relates the intensity of the light at a wavelength of about 830 nm, directly measured by an emission microscope (EMMI), to the substrate current $(I_{\rm sub})$. The photon counts obtained can thus be directly applied to the lifetime-prediction analysis based on the Lucky Electron Model. The method is a development and a simplification of the Photon Emission Method presented by Y. Uraoka and co-workers [4].

II. Optical Measurement of the Substrate Current

One of the effects of hot carriers in saturated Si-MOSFET's is the emission of light over a wide range of wavelengths mainly caused by single-carrier intraband transitions [7]–[9]. This luminescence is spatially concentrated in the high-field regions at the drain end of the channel. Light with an energy higher than the bandgap E_g is significantly reabsorbed within the semiconductor, generating carriers which add to the main contribution of the substrate current $(I_{\rm sub})$ resulting from the primary impact ionization of the hot carriers. Light with an energy closer to E_g can instead propagate in the substrate for several hundred microns. If a reverse biased junction is placed at a convenient distance from the MOSFET, this light can be detected as a reverse current $(I_{\rm coll})$. These two currents have been shown to be in a proportional relation [1], [7], [10]. Part of this light, the one directed toward the surface, can escape from the device and be detected. Its intensity [Photon Count (P.C.)] is therefore proportional to $I_{\rm coll}$ and consequently to $I_{\rm sub}$. A selective measurement of these photons, neglecting the ones with energy lower than E_g that find the

Manuscript received October 9, 1996. The review of this brief was arranged by Editor B. Ricco.

G. Romano is with SGS-THOMSON Microelectronics, 20041 Agrate, Italy.
M. Sampietro is with Politecnico di Milano, Dipartimento Elettronica e Informazione, 20133 Milano, Italy.

Publisher Item Identifier S 0018-9383(97)03019-0.

semiconductor transparent and do not share in producing $I_{\rm coll}$, can therefore be correlated to the degradation of MOS structure.

A. Experimental Apparatus

To confirm the proportionality between Photon Count and $I_{\rm sub}$, we have used an optical microscope with an intensified detector consisting of an extended S-25 photocathode, a micro-channel plate and a CCD. The S-25 extended photocathode is sensitive to photons from ~300 nm up to ~1050 nm (i.e., $1.2\ \text{eV} < E < 5\ \text{eV}$) so that the undesired photons with $E \ll E_g$ are little detected. Bandpass filters from 1000 nm to 600 nm were available to selectively measure photons at a given wavelength. If no filters are used, the intrinsic peak of sensitivity of the system is the trade-off between photocathode sensitivity and emitted light spectrum, in our case at about $E \cong 1.5$ eV ($\cong$ 830 nm).

B. Experimental Analysis

Optical and electrical measurements have been carried out on LDD Si-MOSFET's characterized by a gate length $L = 0.7\ \mu$m, a nominal supply voltage $V_{dd} = 5$ V, low-resistance poly-gate and thin oxide ($\cong$ 17 nm). Fig. 1 shows the photon count and $I_{\rm sub}$ as a function of V_{gs} with V_{ds} constant at 5 V. The curve called "No filter" is obtained operating the EMMI without additional filters. The figure shows that the experimental condition in which the optical measurement better tracks the electrical measurement of $I_{\rm sub}$ is the one in which no filters are used ($\cong$ 830 nm) in good agreement with [6]. At low V_{gs} the photon count with a 600-nm filter is higher than with a 1000-nm filter, while the opposite occurs at high V_{gs}. Other authors, using different photocathodes and therefore "selecting" different wavelengths, have found different relationship between $I_{\rm sub}$ and P.C.: the peaks have been shown to be at a higher V_{gs} [9], at the same V_{gs} [10] or at a lower V_{gs} [11] than the peak of $I_{\rm sub}$. The proportionality between P.C. and $I_{\rm sub}$ when no filter is used is also evidenced in Fig. 2 where the same data are plotted as a function of $I_{\rm sub}$. Only points with "no filter" approximately lie on a straight line, while the linearity is no longer satisfied when other wavelengths are selected (1000 nm or 600 nm), as shown by the two branches of the curves departing from each other. This behavior can be explained considering that the number as well as the energy of the hot carriers at the drain end of the channel vary depending on V_{gs}. As V_{gs} increases, the electric field at the MOSFET drain proportionally decreases, so as the ionization coefficient , while I_{ds} increases. The substrate current and therefore the photon count, proportional to the product $I_{ds} * \alpha$, will reach a maximum for $V_{gs} \cong V_{ds}/2$ and then decrease. The spectrum of the emitted light will change correspondingly, having a significant tail at high energies when the electric field is high (low V_{gs}) and reducing when V_{gs} is close to V_{ds}.

III. Lifetime Prediction Analysis

Thanks to the proportionality between the emitted light and $I_{\rm sub}$, the MOSFET lifetime can be measured directly from an optical measurement. The procedure involves the measurement of the time taken by one parameter of the device under stress to reach a given variation, and the measurement, by means of the EMMI, of the light emitted by the MOSFET in the same stress conditions. Among the device parameters $(g_m, I_{\rm dsat}, V_t)$, we have preferred the oscillation frequency of a ring oscillator (R.O.), that is, the signal propagation delay of the CMOS inverter. In this case, because V_{gs} ranges from 0 V to V_{ds}, each CMOS cell is submitted to a voltage stress similar to the one found in normal operating conditions. The test structures were a 601-CMOS-cell ring, oscillating at a frequency of about 1.9 MHz. The MOSFET's characteristics are the same as specified previously.

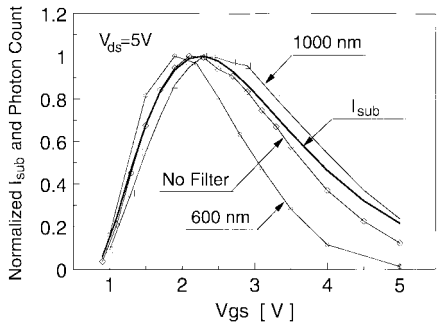

Fig. 1. Normalized substrate current and photon count versus gate voltage. Drain voltage is 5 V. Results show the gate-voltage dependence of the photon count peak as a function of the filter wavelength. "No filter" defines a filter centered at about 830 nm.

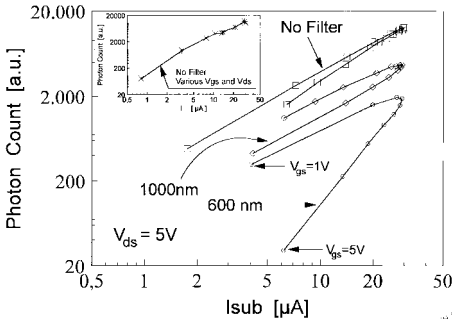

Fig. 2. Photon count of the emitted light versus substrate current when gate voltage varies from $V_{gs} \cong 1$ V to $V_{gs} = 5$ V. The drain voltage is 5 V. Curves refer to three filter wavelengths. The inlet shows that the proportionality between P.C. and $I_{\rm sub}$ stays linear in the case "No filter" also for different values of V_{ds}.

The cells are manufactured with self-aligned twin-tub technology with p-MOSFET wider than n-MOSFET to improve the symmetry between rise and fall transitions. A buffer at the output of the oscillator prevent from loading when frequency is monitored.

A. Measurement of the Degradation Time

The oscillation frequency of a new R.O. is first measured under nominal conditions ($T = 303.0$ K, $V_{dd} = 3.0$ V, lower than the operating 5 V supply voltage in order not to age the device during this measuring step). The R.O is then submitted to stress by biasing it at higher V_{dd} for a given time. Then the R.O. is submitted again to $V_{dd} = 3.0$ V and its oscillation frequency measured. These steps have been repeated until a given threshold of frequency variation has been reached. The results for different values of V_{dd} are shown in Fig. 3. The high sensitivity of the frequency measurement allows to set a low degradation threshold (0.5%) and to perform the experiment in an acceptable time also for weak stressing conditions (for example $V_{dd} = 6$ V).

B. Measurement of the Photon Count

The luminescence that each R.O. under stress produces before reaching the degradation threshold is measured at the same time of the ageing measurement. The EMMI was focused on 10 n-MOSFET's of the ring in order to minimize the errors due to transistor tolerances. Because the light intensity drops drastically when the devices are subject to a weak stress (low V_{dd}) and the photon count is not linearly related to the EMMI acquisition time, the instrument set-up (multiplier gain, acquisition time, number of acquisition, etc.) has been suitably changed during the measurements to always

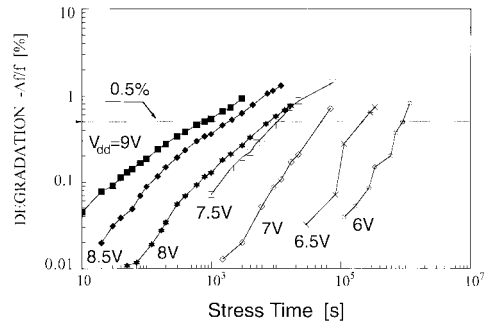

Fig. 3. Frequency shift $\Delta f/f$ of the ring oscillators biased at different stress voltages as a function of stress time.

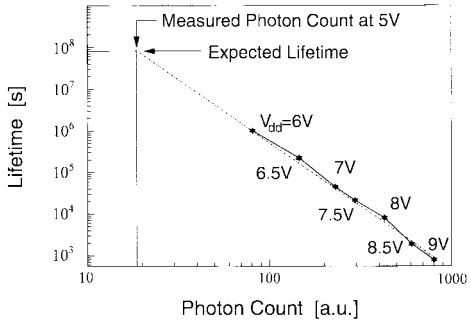

Fig. 4. Plot of the ring oscillator lifetime for different bias voltages. The graph allows to extrapolate the R.O. lifetime at the nominal supply voltage of 5 V or lower.

keep a linear proportionality among measurements. For each value of V_{dd}, the P.C. measurement is plotted with the corresponding value of ageing time in Fig. 4. The alignment along a straight line of the experimental data confirms that the light measured with our experimental set-up is proportional to $I_{\rm sub}$ with a good approximation. The device lifetime under nominal supply voltage can be extrapolated by simply measuring the photon count in the nominal condition. These devices, for example, will reach 0.5% degradation after approximately 925 days of continuous work when operated at 5 V.

IV. Conclusions

The long-term degradation of nMOSFET devices, and therefore of CMOS because pMOSFET degradation is usually negligible, can be studied in their operating condition with good precision to predict their lifetime in the nominal conditions. The procedure and the experimental set-up, based on the monitoring of the oscillation frequency of a ring oscillator and on direct photon count measurements, are simple and could be efficiently introduced as a standard characterization test in production plants. The method differs from that proposed by Uraoka [4] where the lifetime is correlated to the photon count at 200 nm extrapolated by measurements between 400 and 800 nm with the assumption that the energy distribution of the channel electrons is Maxwellian. Actually, light emitted by direct intraband transitions ($E < 2$ eV) and phonon assisted intraband transitions ($E > 2$ eV) have Gaussian spectra and draws a Maxwellian spectrum only in the energy range $1.7 < E < 2.5$ eV because they sum each others [3], [7]. Besides this, Uraoka measurement is more difficult because corrections should be made to the photon count at each wavelength due to the absorption by poly-Si, to the transmittance of the lenses and filters and to the spectral sensitivity of the photon count camera. This should be compared with the simplicity of the method proposed in this paper where the data are directly measured and not extrapolated, the gain of the system is not critical because a relative light measurement is performed and, if a S25 photocathode is used, it is even performed without using a set of filters.

Acknowledgment

The authors would like to thank L. Jacqmin from SGS-Thomson for providing the devices and for his valuable suggestions.

References

[1] C. Hu, S. C. Tam, F. C. Hsu, P. K. Ko, T. Y. Chan, and K. W. Terrill, "Hot-electron-induced MOSFET degradation—Model, monitor, and improvement," *IEEE Trans. Electron Devices*, vol. ED-32, p. 375, Feb. 1985.

[2] K. R. Mistry and B. Doyle, "AC versus DC hot-carrier degradation in n channel MOSFET's," *IEEE Trans. Electron Devices*, vol. 40, p. 96, Jan. 1993.

[3] J. Bude, Sano and A. Yoshii "Hot-carrier luminescence in Si," *Phys. Rev. B*, vol. 45, no. 11, p. 5848, 1992.

[4] Y. Uraoka, N. Tsutsu, T. Morii, and K. Tsuji, "Hot carrier evaluation of MOSFET's in ULSI circuits using the photon emission method," *IEEE Trans. Electron Devices*, vol. 40, p. 1426, Aug. 1993.

[5] L. Selmi, M. Pavesi, H. Wong, A. Acovic, and E. Sangiorgi "A comparative study of hot carriers induced light emission and degradation in bulk and SOI MOSFET's," in Proc. *IEDM Conf.*, 1995, pp. 49.

[6] I. Chonstein, J. Muller, U. Hilleringmann, and K. Goser, "Hot carrier monitoring in nMOS transistors by visible light emission," in *Proc. ESSDERC Conf.*, 1993, pp. 421.

[7] P. A. Childs, R. A. Stuart, and W. Eccleston, "Evidence of optical generation of minority carriers from saturated MOS transistor," *Solid-State Electron*, vol. 26, no. 7, p. 685, 1983.

[8] S. Villa, A. Lacaita, and A. Pacelli "Photon emission from hot electrons in silicon," *Phys. Rev. B*, vol. 52, no. 15, p. 10993, 1995.

[9] T. Tsuchiya and S. Nakajima, "Emission mechanisms and bias-dependent emission efficiency of photons induced by drain avalanche in Si MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-32, p. 405, Feb. 1985.

[10] H. S. Wong, "Experimental verification of the mechanism of hot-carrier-induced photon emission in n-MOSFET's using an overlapping CCD gate structure," *IEEE Electron Device Lett.*, vol. 13, p. 389, Aug. 1992.

[11] A. Toriumi, M. Yoshimi, M. Iwase, Y. Akyima, and K. Taniguchi, "A study of photon emission from n-channel MOSFET's," *IEEE Trans. Electron Devices*, vol. ED-34, p. 1501, July 1987.

Modification of the Einstein Equations of Majority- and Minority-Carriers with Band Gap Narrowing Effect in n-Type Degenerate Silicon With Degenerate Approximation and with Non-Parabolic Energy Bands

Zhi-Xiong Xiao and Tong-Li Wei

***Abstract*—In this brief, a new idea is presented for a modification of Einstein equations of the majority- and minority-carriers with the band gap narrowing effect in an n-type degenerate and uniformly-doped silicon with degenerate approximation and with nonparabolic energy bands. It may imply that the Einstein equation may be one factor for the increase of the minority-carrier diffusion coefficient at high doping levels.**

I. Introduction

Einstein equations of the majority- and minority-carriers are important relations for modern electronic devices. The classical value of the diffusion coefficient to the mobility ratio of the majority- and minority-carriers (hereafter referred to as DMR [1]) is equal to KT/q [2], [3] (where K is Boltzmann constant, T is the absolute temperature, and q is the electronic charge). However, this relation holds only for nondegenerate materials. Its general form of the majority-carrier was first given by Landsberg with degenerate approximation, and it first demonstrated that the DMR depends on carrier concentration under degenerate conditions [4]. Chakravarti and Nag gave a generalized form for the majority-carrier in degenerate semiconductors with nonparabolic energy bands [5]. Later on, a derivative form for DMR of electrons and holes was proposed by Marshak and Van Vliet [6]. Besides, a lot of other papers also discussed DMR at high doping levels under different physical conditions, such as [7]–[9]. Among which, [8] discussed DMR for majority and minority electrons with nonparabolic energy bands for nonuniformly-doped semiconductors and gave an approximation for Fermi integral of order 1/2 with the reduced Fermi level η from 0 to 20, however, this value range of η is not enough at high doping levels, and by comparing the average percent errors in [8] to those in [10], it is shown that the approximation for Fermi integrals in [10] (the relative error is below 1.2% with order from $-1/2$ to 4) are much more accurate (particularly around $\eta = 0$). Besides, the band gap narrowing effect is not considered in all these works.

The Einstein relation of the minority-carrier is seldom discussed at high doping levels. However, a large number of papers have shown experimental results of the minority-carrier mobility in a heavily-doped silicon [11]–[13]. These results show that the minority-carrier mobilities increase with the doping level, but the reason is still not clear.

II. Modification with Degenerate Approximation

In a uniformly-doped sample, the generalized electron Einstein equation can be written as [6]

$$\frac{D_n}{\mu_n} = \frac{1}{q\left(\frac{d\ln n}{dE_{fn}}\right)} \tag{1}$$

where n is the electron concentration. E_{fn} is the electron Fermi energy level. μ_n and D_n are the electron mobility and the diffusion coefficient, respectively.

When the doping concentration N_D is greater than 3×10^{18} cm^{-3}, n can be simply taken as N_D [14]. With the degenerate approximation, n can be written as

$$n = N_D = N_C F_{1/2}\left(\frac{E_{fn} - E'_C}{KT}\right) = N_C F_{1/2}(\eta) \tag{2}$$

where N_C is the effective state density at the bottom of the conduction band. E'_C is the conduction band with the band gap narrowing effect. That is, $E'_C = E_C - \Delta E_{gC}$, where E_C is the conduction band at low doping levels, and ΔE_{gC} is assumed to be the band gap narrowing of the conduction band which can be simply written as $A\Delta E_g$, where ΔE_g is the total band gap narrowing and A is the asymmetry-factor [6]. $F_{1/2}(\eta)$ is the Fermi integral with 1/2 order. As stated already, accurate approximations for $F_j(\eta)$ with different order can be obtained from [10].

With (2), $E_{fn} = \eta KT + E_C - \Delta E_{gC}$, and assuming $\lambda_n = d\Delta E_{gC}/dN_D$, the Einstein equation of the majority electrons can be finally written as

$$\frac{D_n}{\mu_n} = \frac{KT}{q} \times \frac{F_{1/2}(\eta)}{F_{-1/2}(\eta)} \times \frac{1}{1 + \frac{\lambda_n}{\frac{KT}{N_C F_{-1/2}(\eta)} - \lambda_n}}. \tag{3}$$

Equation (3) will reduce to the equation which is shown as (36) in [15] at low doping levels.

Up to now, there are few papers on the Einstein equation of the minority-carrier in the heavily-doped silicon. The hole Einstein equation can be also expressed as [6]

$$\frac{D_p}{\mu_p} = -\frac{1}{q\left(\frac{d\ln p}{dE_{fp}}\right)}. \tag{4}$$

For the minority-carrier concentration is always nondegenerate, its concentration can be written as

$$p = N_V \exp\left(\frac{E'_V - E_{fp}}{KT}\right) \tag{5}$$

where N_V is the effective state density on the top of the valence band. E'_V is the valence band with the band gap narrowing effect. That is, $E'_V = E_V + \Delta E_{gV}$, where E_V is valence band at low doping levels, and ΔE_{gV} is assumed to be the band gap narrowing of the valence band which can be simply written as $(1 - A)\Delta E_g$ [6].

With (5), $E_{fp} = E_{fn}$ at the equilibrium state and assuming $\lambda_p = d\Delta E_{gV}/dN_D$, the Einstein equation of minority holes with the degenerate approximation can be written as

$$\frac{D_p}{\mu_p} = \frac{KT}{q} \times \frac{1}{1 - \frac{\lambda_p}{\frac{KT}{N_C F_{-1/2}(\eta)} - \lambda_n}}. \tag{6}$$

Neglecting the band gap narrowing effect, (6) will reduce to KT/q.

III. Modification With Non-Parabolic Energy Bands

In the previous section, the deductions are based on parabolic energy bands, however, it is more accurate to assume that energy bands are nonparabolic.

When N_D is greater than 3×10^{18} cm^{-3} and with nonparabolic energy bands, the effective majority-carrier concentration should be

Manuscript received October 9, 1995; revised August 26, 1996. The review of this brief was arranged by J. R. Hauser.

Z.-X. Xiao is with the Institute of Microelectronics, Peking University, Beijing 100871, P.R.O.C.

T.-L. Wei is with the Microelectronics Center, Southeast University, Nanjing 210018, P.R.O.C.

Publisher Item Identifier S 0018-9383(97)02379-4.

expressed as [5], [6]

$$n = N_D = N_C[F_{1/2}(\eta) + s \cdot F_{3/2}(\eta)] \qquad s = 15KT\alpha/4 \tag{7}$$

where $\alpha = 1/(E_g - \Delta E_{gC} - \Delta E_{gV}) = 1/(E_g - \Delta E_g)$.

With substituting (7) into (1), the Einstein equation for majority electrons with nonparabolic energy bands can be finally written as (8), shown at the bottom of the page.

If the band gap narrowing effect is neglected, (27) will reduce to a familiar equation, such as (10) in [1] and (10) in [5].

At the equilibrium state and with nonparabolic energy bands, the Einstein equation of minority holes can be deduced as

$$\frac{D_p}{\mu_p} = \frac{KT}{q}\frac{1}{1 - \frac{\lambda_p}{B}}. \tag{9}$$

Neglecting the band gap narrowing effect, (9) will reduce to KT/q.

The shifts of the conduction band and the valence band in n-type doped silicon can be obtained by [16].

IV. Discussion

References [11]–[13] have given experimental results of the diffusion length L and the lifetime τ of the minority-carrier, and the calculated mobility values in the heavily-doped silicon. The results show that the minority-carrier mobility increases with the doping level in the heavily-doped silicon. The mobility values are obtained as

$$\mu = (q/KT)[L^2/\tau]. \tag{10}$$

Obviously, the Einstein equation has been simplified to be KT/q, but if (6) or (9) is considered, the experiments may only mean that the diffusion coefficient increases with the doping level. Reference [17] has given the calculation of the minority-carrier mobility which shows that the mobility slightly increases with the doping level at high concentrations. Equations (6) and (9) may imply that the Einstein equation may be another factor for the increase of the minority-carrier diffusion coefficient at high doping levels.

V. Conclusion

With considering the band gap narrowing effect, the Einstein equations of the majority- and minority-carriers have been modified in the n-type degenerate and uniformly-doped silicon with the degenerate approximation and with nonparabolic energy bands. It may imply that the Einstein equation may be one factor for the increase of the minority-carrier diffusion coefficient at high doping concentrations.

References

[1] K. P. Ghatak and M. Mondal, "The diffusivity-mobility ration in nonparabolic materials," *J. Appl. Phys.*, vol. 71, pp. 1277–1283, 1992.

[2] B. R. Nag, *Electron Transport in Compound Semiconductors*. Berlin, Germany: Springer, 1980.

[3] S. M. Sze, *Physics of Semiconductor Devices*. New York: Wiley, 1969, p. 40.

[4] P. T. Landsberg, "On the diffusion theory of rectification," in *Proc. Roy Soc. A*, 1952, vol. 213, p. 226.

[5] A. N. Chakravarti and B. R. Nag, "Generalized Einstein relation for degenerate semiconductors having nonparabolic energy bands," *Int. J. Electron.*, vol. 37, p. 281, 1974.

[6] H. Marshak and C. M. Van Vilet, "Electrical current and carrier density in degenerate materials with nonuniform band structure," in *Proc. IEEE*, 1984, vol. 72, pp. 148–164.

[7] S. N. Mohammad, "Fermi energy and Fermi-Dirac integrals for zinc blende-symmetry narrow-gap semiconductors with spherical energy bands," *J. Phys. C.*, vol. 13, p. 2685, 1980.

[8] S. N. Mohammad and A. V. Bemis, "The Einstein relation for degenerate semiconductors with nonuniform band structures," *IEEE Trans. Electron Devices*, vol. 39, pp. 2826–2828, 1992.

[9] S. N. Mohammad and S. T. H. Abidi, "Theory of saturation photocurrent and photovoltage in p-n junction solar cell," *J. Appl. Phys.*, vol. 61, p. 4909, 1987.

[10] X. Aymerich-Humet, F. Serra-Mestres, and Millán, "A generalized approximation of the Fermi–Dirac integrals," *J. Appl. Phys.*, vol. 54, pp. 2850–2851, 1983.

[11] C. H. Wang, K. Misiakos, and A. Neugroschel, "Temperature dependence of minority hole mobility in heavily-doped silicon," *Appl. Phys. Lett.*, vol. 5, pp. 159–161, July 1990.

[12] C. H. Wang and A. Neugroschel, "Minority-carrier transport parameters in degenerate n-type silicon," *IEEE Electron Device Lett.*, vol. 11, pp. 576–578, Dec. 1990.

[13] I.-Y. Leu and A. Neugroschel, "Minority-carrier transport parameters in heavily-doped p-type silicon at 296 and 77 K," *IEEE Trans. Electron Devices*, vol. 40, p. 1872, 1993.

[14] C. Kittel, *Introduction to Solid-State Physics*. New York: Wiley, 1971, p. 723.

[15] M. Chrzanowska-Jeske and R. C. Jaeger, "BILOW-Simulation of low temperature bipolar device behavior," *IEEE Trans. Electron Devices*, vol. 36, pp. 1475–1489, 1989.

[16] J. R. Lowney and H. S. Bennet, "Effect of donor impurities on the conduction and valence bands of silicon," *J. Appl. Phys.*, vol. 53, pp. 433–438, 1982.

[17] D. B. M. Klaassen, "A unified mobility model for device simulation—Part II: Temperature dependence of carrier mobility and lifetime," *Solid-State Electron.*, vol. 35, pp. 961–967, 1992.

$$\frac{D_n}{\mu_n} = \frac{KT}{q} \times \frac{F_{1/2}(\eta) + sF_{3/2}(\eta)}{[F_{-1/2}(\eta) + sF_{1/2}(\eta)] + [F_{-1/2}(\eta) + sF_{1/2}(\eta) + s\alpha KTF_{3/2}(\eta)]\frac{\lambda_n}{B} + s\alpha KTF_{3/2}(\eta)\frac{\lambda_p}{B}}$$

$$B = \frac{dE_{fn}}{dN_D} = \frac{KT[1/N_C - (\lambda_n + \lambda_p)\alpha sF_{3/2}(\eta)]}{F_{-1/2}(\eta) + sF_{1/2}(\eta)} - \lambda_n. \tag{8}$$