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Base etched selfaligned transistor technology for advanced polyemitter bipolar transistors

M.J. Kumar and D.J. Roulston

Indexing terms: Bipolar transistors, Semiconductor devices

The authors report the fabrication of double selfaligned advanced bipolar transistors using base etched selfaligned transistor technology (BESTT). The main feature of these transistors is that the base and emitter contacts are self-aligned although using only a single poly layer. The fabrication and DC electrical measurements are discussed.

Introduction: The application of the polysilicon emitter to bipolar transistors has resulted in a number of improvements in the device performance [1–3] and forms the basis of most advanced commercially used transistors [4]. However, because simple structures of these transistors have parasitic regions leading to performance degradation, it is desirable to use selfaligned structures to achieve high-speed operation and high packing density. In this Letter we report the successful application of the base etched selfaligned transistor technology [5, 6] for fabricating double selfaligned advanced bipolar transistors. The important advantage of the BESTT process is that it yields a minimum area transistor, because only a single polysilicon layer is used and both the base and emitter contacts are selfaligned. Most double selfaligned transistors use two polysilicon layers; one for the shallow emitter and the other for the base electrode. The base polysilicon should be etched away to open the emitter diffusion window. This etching process increases the transistor failure rate [7] as a result of the collector-emitter leakage current caused by crystal damage during etching. Because the BESTT transistors use only a single poly layer, the active emitter region is free from such damage.

Device fabrication: The BESTT structures were fabricated on wafers with an n-type epitaxial layer of $10^{16}/cm^3$ doping and 1.5 μm thickness. A schematic diagram of the BESTT transistor cross-section is shown in Fig. 1. The base region was formed by implanting boron through a 200Å screen oxide at 20keV and at a dose of $2\times10^{13}/cm^2$. Emitter windows were opened and this was

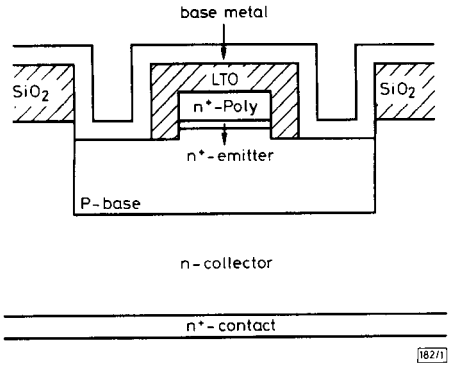

Fig. 1 *Schematic cross-section of BESTT structure*

followed by an RCA cleaning. Next a 0.3μm thick undoped polysilicon region was deposited at 584°C and was implanted with arsenic at 120keV at a dose of $2\times10^{16}/cm^2$. This was followed by an undoped LTO layer deposition at 400°C. The LTO layer was first patterned in buffered HF and using this as a mask, the n^+ doped poly layer was patterned in an aqueous KOH solution. Immediately after the poly was cleared, the KOH etching was stopped and ~500Å of silicon in the base contact windows was etched by a controlled reactive ion etching in SF_6 and O_2 plasma. This particular step is needed to make sure that the base contact is made below the emitter-base junction so that the sideways diffusion of impurities from the extrinsic p^+ base implantation does not short the e-b junction. A rapid thermal annealing at 900°C was then performed for 30min to activate the dopants and also to drive-in the arsenic to form the emitter junction. Another layer of LTO was then deposited and an unmasked reactive ion etching was carried out in CF_4 and H_2/He plasma. Because this is an anisotropic etching, it leaves a sidewall oxide on the polysilicon emitter while clearing the oxide from the base contact regions. Opening of emitter contact windows was followed by aluminum deposition. A rapid thermal annealing at 250°C in N_2 and H_2 completed the device.

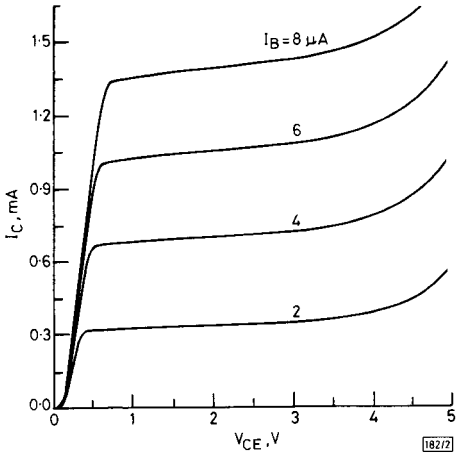

Fig. 2 *Measured $I_C - V_{CE}$ characteristics of BESTT structure (emitter area is $2\times3\ \mu m^2$)*

Device characteristics: The measured $I_C - V_{CE}$ characteristics of a BESTT transistor with a $2\times3\mu m^2$ emitter area are shown in Fig. 2. The breakdown voltage BV_{ceo} is approximately 6V. The Gummel plots for the same device are shown in Fig. 3 and are compared with the BIPOLE simulation results. The base and collector currents do not cross each other, indicating that the surface recombination at the sidewall oxide around the n^+ doped polyemitter is not significant. The measured and BIPOLE simulated DC current

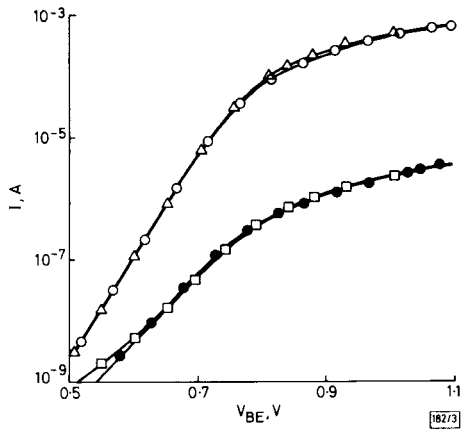

Fig. 3 *Gummel plots of BESTT structure (emitter area is 2×3 μm²)*

● Measured I_B
□ Simulated I_B
○ Measured I_C
Δ Simulated I_C

gain β is plotted in Fig. 4 as a function of collector current. The peak current gain is ~200. Based on the Gummel plots and the β against I_C measurements, we have obtained an accurate fitting for the emitter and base doping profiles using BIPOLE. We have also verified the collector doping from the capacitance-voltage measurements. The emitter and base junction depths, estimated using BIPOLE, are 0.040 and 0.14μm, respectively. Our simulation results show that these transistors have a peak f_t of ~8GHz as shown inset in Fig. 4.

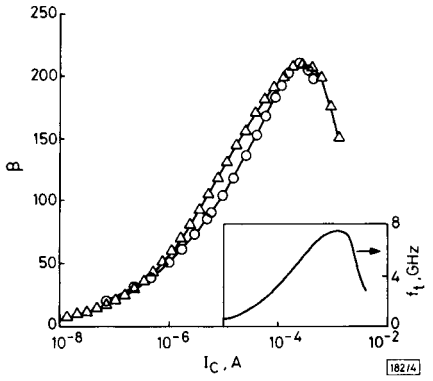

Fig. 4 *β against I_C of BESTT structure (emitter area is 2×3 μm²)*

○ Measured β
Δ Simulated β
Inset: Simulated f_t against I_C of the same device

We have also fabricated non-selfaligned structures on the same wafer for a comparison of reduction in parasitic capacitances. The measured zero bias e-b capacitance of the BESTT structure is 3.4×10^{-7}F/cm² and that of the non-selfaligned structure is 7.2×10^{-7}F/cm². In the latter case, the extra capacitance arises due to the overlapping of the polysilicon emitter on the oxide in the base window which is inevitable in non-self-aligned structures. In the BESTT structure, the spacing from the edge of the emitter area to the base electrode is determined only by the width of the sidewall oxide and will therefore result in a smaller base resistance compared to the non-selfaligned device. The maximum frequency of oscillation f_{max} of the BESTT structure is expected to be higher because of the reduced base resistance and the smaller parasitic capacitance.

Conclusion: We have demonstrated the application of base etched selfaligned transistor technology for the fabrication of double selfaligned advanced bipolar transistors with very shallow junction depths. The fabrication and electrical characteristics of these transistors were discussed.

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Electrical properties and thermal stability of MBE-grown Al/$Al_xGa_{1-x}As$/$Al_{0.25}Ga_{0.75}As$ Schottky barriers

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Indexing terms: Schottky-barrier diodes, Molecular beam epitaxial growth

The effects of the Al mole fraction of a thin (4nm) $Al_xGa_{1-x}As$ cap on the barrier height and the thermal stability of Al/$Al_xGa_{1-x}As$/$Al_{0.25}Ga_{0.75}As$ Schottky barriers prepared *in situ* by MBE have been investigated. The behaviour of the barrier heights and the ideality factors of diodes after annealing up to 435°C are studied.

Introduction: The barrier height and the thermal stability of $Al_xGa_{1-x}As$ Schottky barriers used as gate contacts play an important role in determining the performances and the reliability of devices such as MESFETs and HEMTs. Nevertheless, only a few studies have been reported on metal/AlGaAs junctions [1, 2], mainly because the high surface reactivity of the ternary alloy makes it difficult to control the surface before the metal deposition. Thus, the most reliable studies were carried out on Al/*n*-AlGaAs diodes prepared *in situ* by MBE, i.e. when oxide free interfaces were obtained. These studies show a strong dependence of the barrier height on the AlAs mole fraction [1–3] while very lit-