

Collector Recombination Lifetime from the Quasi-Saturation Analysis of High-Voltage Bipolar Transistors

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Abstract—It is shown that the collector recombination lifetime can be evaluated accurately by extending the quasi-saturation analysis of high-voltage bipolar transistors into the high-current regime. It is demonstrated experimentally that the values of lifetime obtained by the present method are independent of emitter region recombination effects.

I. INTRODUCTION

RECENTLY it has been shown that the collector recombination lifetime plays an important role in modeling high-voltage bipolar transistors operating in quasi-saturation [1]. This lifetime is generally measured by the well-known Open Circuit Voltage Decay (OCVD) technique [2] using the collector-base junction and leaving the emitter floating. A recent study has shown that [3] the collector lifetime measured by this technique is considerably influenced by the presence of the floating emitter. Similar results on the dependence of OCVD lifetime on emitter region properties have been reported in literature [4]. Consequently, as demonstrated in [3], the OCVD method can be used to determine the collector region lifetime τ_v correctly, only if the emitter region is etched away completely. This limitation of the method prevents the use of OCVD technique on completed devices.

In this paper, therefore, a novel method of measuring the collector recombination lifetime, which is independent of emitter effects, is presented by extending the quasi-saturation analysis of high-voltage bipolar transistors [1] to the high-current density regime. The technique is supported by adequate theory and the experimental results are presented on transistors fabricated with different emitter properties.

II. THEORY

Considering an $n^+ - p - \nu - n^+$ transistor, shown in Fig. 1, the common emitter current gain h_{FE} in quasi-saturation region can be written as [1]

$$h_{FE} = \frac{h_{FE0}}{1 + \left[\frac{1 + h_{FE0}}{4D_{nc}\tau_v} + \frac{I_C}{4D_{nc}^2 A_v (Q_B/D_{nB})} \right] x'^2} \quad (1)$$

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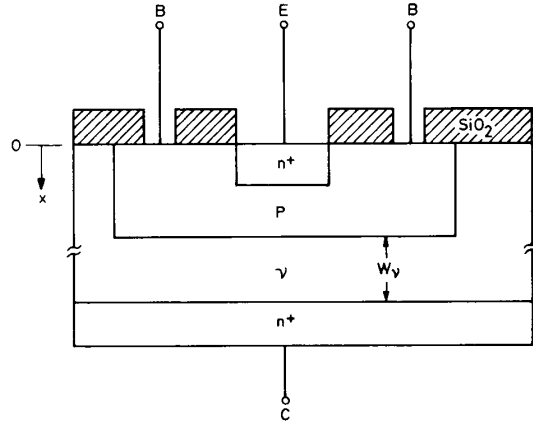


Fig. 1. The structure of the high-voltage bipolar transistors fabricated in the present study.

where h_{FE0} is the common emitter current gain in the active region, I_C is the collector current, τ_v is the collector recombination lifetime, D_{nc} is the average diffusion coefficient of electrons in the ν -region, and (Q_B/D_{nB}) is the base Gummel number. A_v is the effective ν -region area. When the transistor is operating in the quasi-saturation region, the collector-base junction is forward-biased. Consequently, the hole injection to the ν -region takes place over the entire collector-base junction. Hence, the effective area A_v can be taken to be the actual collector area. x' is the width of the conductivity modulated region in the collector and is given by

$$x' = W_v - \frac{V_{CER} A_v}{I_C \rho_v} \quad (2)$$

where W_v is the width of the collector ν region and V_{CER} is the voltage drop in the collector ν region of width $(W_v - x')$ which is not conductivity modulated [1]; ρ_v is the collector region resistivity and is given by

$$\rho_v = \frac{1}{q\mu_0 N_v} \quad (3)$$

where μ_0 is the low-level electron mobility and N_v is the doping density in the collector ν region. Using (3) in (2),

x' can be written in the following form:

$$x' = W_v \left[1 - \frac{I_0}{I_C} \right]. \quad (4)$$

Here I_0 is the threshold current for quasi-saturation to set in and is expressed as

$$I_0 = \frac{q\mu_0 N_v A_v V_{CER}}{W_v}. \quad (5)$$

Inserting (4) and (5) in (1), we get

$$h_{FE} = \frac{h_{FE0}}{1 + \frac{Q'}{\tau_v} + \frac{Q_0 D_{nB}}{Q_B D_C^*} \left(\frac{I_C}{I_0} + \frac{I_0}{I_C} - 2 \right)} \quad (6)$$

where

$$Q' = \frac{(1 + h_{FE0}) W_v^2}{4D_{nc}} \left[1 - \frac{I_0}{I_C} \right]^2 \quad (7)$$

$$Q_0 = \frac{V_{CER}}{4kT/q} N_v W_v \quad (8)$$

$$D_C^* = \frac{D_{nc}^2}{D_0}. \quad (9)$$

Here

$$D_0 = \mu_0 (kT/q).$$

At high current densities, i.e., when $I_C \gg I_0$, the value of x' in (4) approaches W_v and (7) reduces to

$$Q' = \frac{(1 + h_{FE0}) W_v^2}{4D_{nc}}. \quad (10)$$

Using (5) and (7)–(10) in (6), the current gain h_{FE} at high current densities can be written as

$$h_{FE} = \frac{h_{FE0}}{\left(1 + \frac{Q'}{\tau_v} \right) + \frac{I_C W_v^2}{4q(Q_B/D_{nB}) D_{nc}^2 A_v}}. \quad (11)$$

It is clear from (11) that the collector current I_C can be related to h_{FE} as follows:

$$I_C = \frac{Q h_{FE0}}{h_{FE}} - Q \left[1 + \frac{Q'}{\tau_v} \right] \quad (12)$$

where

$$Q = \frac{4q(Q_B/D_{nB}) D_{nc}^2 A_v}{W_v^2}. \quad (13)$$

It can be seen from (12) that a plot of I_C versus $1/h_{FE}$ should give a straight line with a slope equal to $Q h_{FE0}$ and the Y axis intercept equal to $Q(1 + Q'/\tau_v)$. The recombination lifetime τ_v can now be extracted from the intercept of this straight line if the other physical parameters of the transistor are known. It is important to note here that (12) is valid only when $I_C \gg I_0$.

III. EXPERIMENTAL RESULTS AND DISCUSSION

To examine the usefulness of the present analysis for extracting the collector recombination lifetime, n^+ - p - v - n^+ transistors are fabricated using planar technology. The structure of the transistors fabricated is shown in Fig. 1. Typical emitter–base junction depth, in these transistors, is 1.16 μm and the base–collector junction depth is 3.3 μm . Measurements are carried out on two sets of devices, viz., set *A* and set *B*. Set *A* corresponds to transistors with the full emitter present. The transistors in set *B* are obtained by etching the emitter to a depth of 0.65 μm from the surface by anodization and stripping the oxide. Thus the transistors in set *A* and set *B* are identical in all other respects. The measured parameters of these transistors are given in Table I. By keeping $V_{CE} = 5$ V, the current gain h_{FE} in quasi-saturation is measured at different collector currents on a number of transistors of set *A* and set *B*. These results are shown in Fig. 2(a) in the form of I_C versus $1/h_{FE}$. It can be seen that these plots turn out to be straight lines for values of $I_C \gg I_0$, I_0 being less than 0.1 mA for $V_{CER} < 5$ V. V_{CER} is slightly less than V_{CE} due to the emitter base drop V_{BE} , collector base drop V_{CB} , the voltage drop V_{ox} across the conductivity modulated v region, and $I_C R_{sat}$ drop. The V_{CER} values are computed by taking into account these voltage drops. I_0/I_C in (3) is then estimated as a function of I_C to obtain x' versus I_C , shown in Fig. 2(b). Here, it can be seen that x' approaches W_v for $I_C > 3$ mA, i.e., for $I_C/I_0 \gg 1$. Below this current x' is considerably smaller than W_v and (12) is not valid. The experimental results shown in Fig. 2(a) thus deviate from the straight-line behavior when I_C becomes comparable to I_0 . The straight-line portions obtained on the two sets of transistors, for collector currents greater than 3 mA, are extrapolated to intersect the Y axis and the intercepts are used for estimating the collector lifetime τ_v . Thus if C is the intercept on the Y axis in Fig. 2(a), the collector recombination lifetime τ_v can be written from (12) and (13) as

$$\tau_v = \frac{(1 + h_{FE0}) W_v^2}{4D_{nc}} \left[\frac{C W_v^2}{4q(Q_B/D_{nB}) D_{nc}^2 A_v} - 1 \right]^{-1}. \quad (14)$$

The parameters required in (14) are given in Table I for the transistors used in the present analysis. The value of the average diffusion coefficient D_{nc} in (14) is 24 cm^2/s and is determined as described in literature [1]. The values of recombination lifetime τ_v for the transistors of set *A* and set *B* having different emitter junction depths are thus extracted using (14) and the Y axis intercepts in Fig. 2(a). These values of τ_v are found to be equal to 13.2 μs for the transistors of set *A* as well as set *B*, thus showing that the collector lifetime τ_v is independent of the differences in the emitter regions.

It may be noted that (14) for τ_v is valid when the measurements are carried out at sufficiently large I_C such that $I_C \gg I_0$. Under these circumstances, as can be seen from Fig. 2(b), $x' \cong W_v$ and hence the results are independent

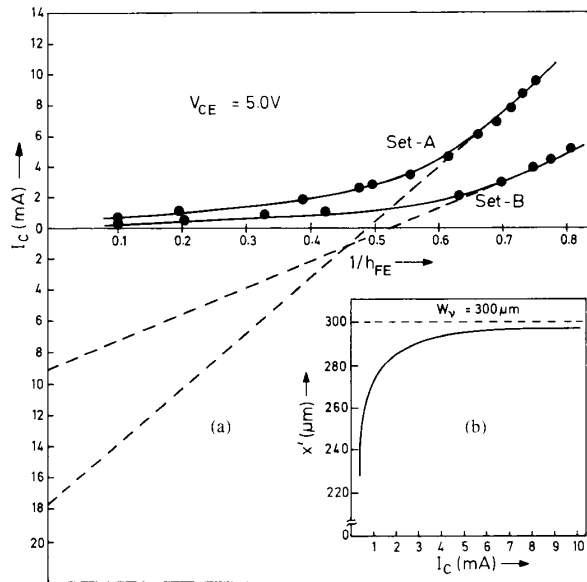


Fig. 2. (a) The experimental I_C versus $1/h_{FE}$ plots for the n^+p-n^+ transistors fabricated in this study. (b) The width x' of the conductivity modulated ν region as a function of collector current I_C .

TABLE I
MEASURED PARAMETERS OF THE TRANSISTORS

Parameter	set A	set B
	Full emitter present	Emitter etched upto $0.65 \mu\text{m}$ from surface
Thickness of emitter etched from surface X_R	$0.0 \mu\text{m}$	$0.65 \mu\text{m}$
Emitter-base junction depth X_j	$1.16 \mu\text{m}$	$0.51 \mu\text{m}$
Current gain in the active region h_{FE0}	100	52
Effective collector ν -region area A_ν	$6.25 \times 10^{-4} \text{cm}^2$	$6.25 \times 10^{-4} \text{cm}^2$
Base Gummel number Q_B/qD_{nB}	$1 \times 10^{12}/\text{cm}^{-4} - \text{sec}$	$1 \times 10^{12}/\text{cm}^{-4} - \text{sec}$
Thickness of collector ν -region	$300 \mu\text{m}$	$300 \mu\text{m}$

of V_{CE} . Our own measurements have indeed shown that the measured τ_ν is independent of V_{CE} .

For the purpose of comparison, lifetime measurements are carried out using OCVD technique on the collector-base junctions of transistors in set A and set B, leaving the emitter floating. For the transistors of set A where the full emitter is present, the value of OCVD lifetime $\tau_{\nu(\text{eff})}$

TABLE II
COMPARISON OF MEASURED LIFETIMES

Transistor sets	Lifetime values obtained by OCVD technique	Lifetime values obtained using present analysis
set A Full emitter present	$10.0 \mu\text{sec}$	$13.2 \mu\text{sec}$
set B Emitter etched upto $0.65 \mu\text{m}$ from the surface	$7.0 \mu\text{sec}$	$13.2 \mu\text{sec}$
Collector-base junction of transistors with the emitters completely etched out	$12.5 \mu\text{sec}$	—

is found to be $10 \mu\text{s}$. In set B, where $0.65 \mu\text{m}$ of the emitter is etched out, the value of OCVD lifetime $\tau_{\nu(\text{eff})}$ is $7 \mu\text{s}$. This reduction in the OCVD lifetime with emitter etching is due to an increase in the injected hole current into the emitter [3], [5]. However, as pointed out in [3], the true value of collector lifetime can be obtained by the OCVD technique only by completely etching the emitter and measuring the lifetime on the collector-base junction. The value of τ_ν thus measured for the transistors of the present study is $12.5 \mu\text{s}$.

The collector recombination lifetime obtained on the transistors in set A and set B using OCVD technique and the present approach are compared in Table II. As can be noted from here, the value of τ_ν obtained by the present technique does not change with emitter thickness and is thus independent of emitter region effects. This value is also close to the lifetime obtained by the OCVD technique on the collector-base junction of the transistors whose emitter region is completely etched out, thus demonstrating the validity of extracting τ_ν using the present method.

IV. CONCLUSIONS

It is demonstrated in this work that the collector recombination lifetime τ_ν can be extracted very conveniently by extending the quasi-saturation analysis of high-voltage bipolar transistors [1] into high-current regime. This is a nondestructive method and gives the lifetime values at the current densities normally encountered when the transistor is in actual operation. It is further shown that the values of τ_ν obtained by the present method are independent of the properties of the emitter region.

REFERENCES

- [1] K. N. Bhat, M. J. Kumar, V. Ramasubramanian, and P. George, "The effects of collector lifetime on the characteristics of high voltage bipolar transistors operating in the quasi-saturation region," *IEEE Trans. Electron Devices*, vol. ED-34, pp. 1163-1169, May 1987.
- [2] P. G. Wilson, "Recombination in silicon p- π -n diodes," *Solid-State Electron.*, vol. 10, pp. 145-154, 1967.
- [3] M. J. Kumar and K. N. Bhat, "The effects of emitter region recombination and bandgap narrowing on the current gain and the collector

lifetime of high voltage bipolar transistors," *IEEE Trans. Electron Devices*, vol. 36, pp. 1803-1810, Sept. 1989.

- [4] P. L. Hower, "Bipolar transistors," in *Semiconductor Devices for Power Conditioning*, R. Sittig and P. Roggwiller, Eds. New York, NY: Plenum, 1982, pp. 273-306.
- [5] M. J. Kumar, "High voltage bipolar transistor device modeling including the collector region recombination and the emitter region heavy doping effects," Ph.D. dissertation, Dep. Elec. Eng., Indian Institute of Technology, Madras, India, July 1989.

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