Pergamon

0038-1101(95)00091-7

Solid-State Electronics Vol. 38, No. 10, pp. 1854–1856, 1995

0038-1101/95 $9.50 + 0.00

NOTE

NEW BURIED P^+-GRID POLYSILICON EMITTER BIPOLAR POWER TRANSISTOR

(Received 5 October 1994; in revised form 17 February 1995)

INTRODUCTION

Besides quasi-saturation effects[1,2], emitter current crowding is one of the most important criteria in the design of bipolar power transistors[3,4]. When emitter crowding occurs, most of the emitter current flows along the emitter periphery into the lightly doped base region, leaving most of the central emitter area inactive. This is a result of the transverse voltage drop from the center of the emitter to the base contact caused by transverse flow of base current[5,6]. One common solution to reducing the transverse base resistance and hence the emitter current crowding is to use several emitter stripes alternating with base contact stripes, known as an interdigitated structure[7]. However, the disadvantage of this approach is that it results in a poor silicon surface utilization due to the extra space required between the emitter and base stipes imposed by lateral diffusion and lithographic constraints.

In this paper, we propose a novel polysilicon emitter bipolar power transistor structure using a buried P^+ grid in the base region directly under the emitter. Unlike conventional power transistors, the base current in this proposed structure is uniformly spaced across the lightly doped base region by means of a buried P^+ grid created by ion implantation. As a result, the base current in this structure does not have to flow through a significant horizontal base resistance in order to inject carriers into the emitter. Another important advantage of this novel structure is that the surface area of the emitter is more efficiently utilized because here the emitter need not be interdigitated with such narrow emitter stripes as would otherwise be required.

BURIED P^+ GRID

A schematic of the device structure and the corresponding grid pattern are shown in Fig. 1 where L_{p^-} is the width of the ion implanted buried P^+ grid stripe and L_{base} is the width of the active part of the lightly doped base region. Conventional planar technology can be used to fabricate this structure except that it needs an additional mask level to implant the P^+ grid by opening windows in the oxide grown in the base window during base drive-in. The buried P^+ grid transistor structures were fabricated on $\langle 111 \rangle$ bulk n-type wafers of 40–60 Ω-cm resistivity and 270–300 μm thickness. First, an n^+ contact region was created on unpolished back surface by phosphorus diffusion. The base region was formed by (i) predepositing boron at 900°C for 15 min and (ii) boron glass removal and drive-in at 1100°C for 15 h. Windows were opened in the base region and boron was implanted at 200 keV at a dose of $10^{15}/cm^2$ to create the P^+ grids. This was followed by rapid thermal annealing at 900°C to activate the boron impurities. Emitter windows were next opened and this was followed by an RCA clean to form a thin layer of native oxide[8]. Next a 0.3 μm thick undoped polysilicon layer was deposited at 584°C and was implanted with arsenic at 100 keV at a dose of $2 \times 10^{16}/cm^2$. This was followed by an undoped LTO layer deposition at 400 C. The LTO layer was first patterned in buffered HF and using this as a mask, the n^+ doped poly layer was patterned in an aqueous KOH solution. This was again followed by an undoped LTO layer deposition at 400°C. Now a rapid thermal annealing at 900°C was performed for 30 min to activate the dopants and also to drive-in the arsenic from the polysilicon into single crystal silicon to form the emitter junction. Opening emitter contact windows was followed by aluminum deposition. A rapid thermal anneal at 250°C in N_2 and H_2 completes the device.

We fabricated four test patterns having: (i) a buried P^+ grid with $L_{p^-} = 5\ \mu m$, $L_{base} = 5\ \mu m$. Here, the number of L_{p^+} and L_{base} regions under the emitter is 100 each and therefore corresponds to 50% active base area; (ii) with $L_{p^-} = 5\ \mu m$, $L_{base} = 10\ \mu m$ and 67 each of L_{p^-} and L_{base} regions under the emitter or 66.66% active base area; (iii) with $L_{p^-} = 5\ \mu m$, $L_{base} = 15\ \mu m$ and 50 each of L_{p^-} and L_{base} regions under the emitter or 75% active base area; (iv) a conventional base with no buried P^+ grid under the emitter and therefore 100% active base area. In all our calculations we assume that the lateral diffusion of P^+ fingers after RTA treatment is negligible and that the P^+ finger width remains the same as the mask dimensions of the grid after annealing.

The doping profiles of the buried P^+ grid transistors obtained using SUPREM III for the above process are shown in Fig. 2. The emitter–base junction depth is 0.04 μm and the base–collector junction depth is 6.2 μm. The implantation parameters for the buried P^+ grid are chosen

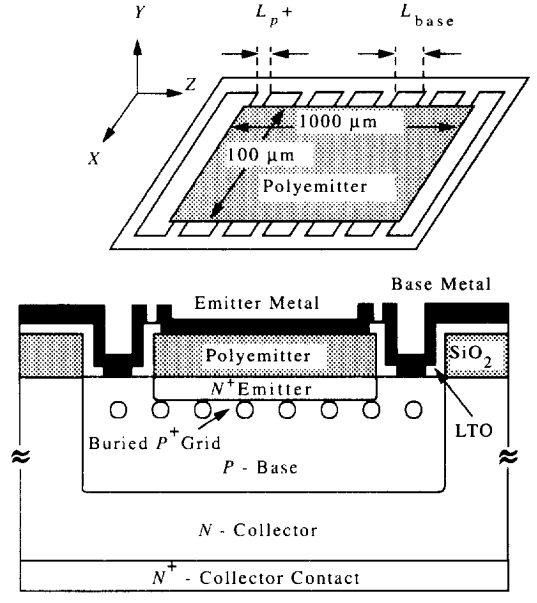

Fig. 1. Schematic cross-section of the buried P^+ grid polyemitter bipolar power transistor.

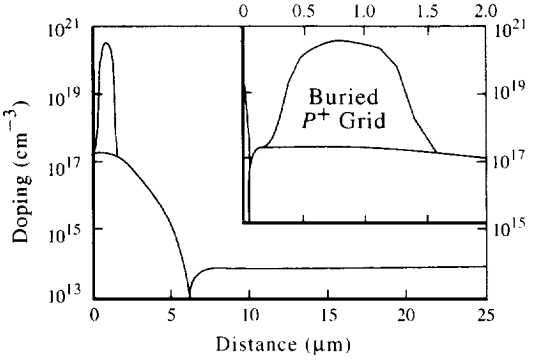

Fig. 2. Doping profiles of the transistors obtained using SUPREM III.

such that the peak of the implantation lies underneath the emitter with a small space separating its tail and the emitter–base junction as shown in the inset of Fig. 2. Since the L_{p^+} grid stripes are connected in parallel, the effective resistance of this grid will be very small and the base current can now spread uniformly under the emitter which is in effect similar to having an interdigitated emitter.

REDUCTION IN BASE RESISTANCE

The base region with a buried P^+ grid under the emitter can be considered as a series of resistances (due to alternating P^+ buried stripe and lightly doped base region) connected in parallel as shown in Fig. 1. Since the base resistance is a result of the horizontal flow of base current under the emitter in the base region, its value is a function of the doping level and thickness of the neutral base region, together with the horizontal dimensions of the active base region[5,6]. When the buried P^+ grid is present, the effective base resistance $R_{BB(eff)}$ to the base current in the x-direction is determined by the density of the P^+ grid stripes and the doping in the active base region under the emitter and is given by:

$$R_{BB(eff)} = \frac{1}{n} \cdot \frac{R_{px} \cdot R_{p^+x}}{R_{px} + R_{p^+x}}, \qquad (1)$$

where n is the number of L_{base} or L_{p^-} stripes, R_{px} is the base resistance of L_{base} in the x-direction and R_{p^+x} is the base resistance of stripe L_{p^-} in the x-direction.

To study the effect of the density of P^+ grid lines under the emitter on the effective base resistance $R_{BB(eff)}$, we have varied the number of P^+ grid lines by keeping the width L_{p^-}

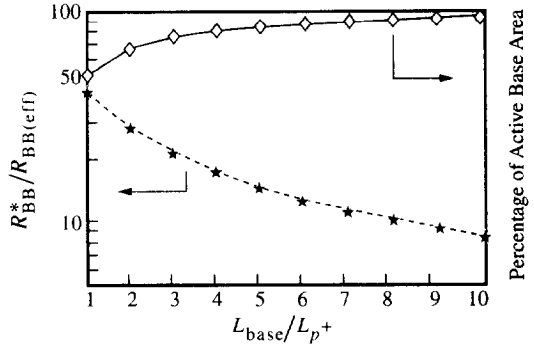

Fig. 3. The active base area (solid line) and the values of $R^*_{BB}/R_{BB(eff)}$ (broken line) as a function of L_{base}/L_{p^-}. R^*_{BB} is the base resistance when no buried P^+ grid is present under the $100 \times 1000\,\mu$m emitter. $R_{BB(eff)}$ is the effective base resistance with the buried P^+ grid.

fixed at $5\,\mu$m. As an illustration, if we take $L_{p^-} = L_{base}$, we can have 100 each of L_{p^-} and L_{base} under the $100 \times 1000\,\mu$m emitter shown in Fig. 1. In this case, the active base area contributing to the current gain of the transistor is only 50% of the total base area under the emitter. Similarly, if L_{base} is 3 times L_{p^+}, we can have 50 each of L_{p^+} and L_{base} under the emitter and the active base area is 75%. In our study, we have varied L_{base}/L_{p^+} between 1 and 10. For each of these cases we have estimated R_{px} and R_{p^+x} in eqn (1) using BIPOLE3 [9] for the doping profiles shown in Fig. 2. When no buried P^+ grid is present under the $100 \times 1000\,\mu$m emitter, the value of the base resistance R^*_{BB} in the x-direction obtained using BIPOLE3 is $3.9\,\Omega$. The values of $R^*_{BB}/R_{BB(eff)}$ and the effective base area as a function of L_{base}/L_{p^-} are plotted in Fig. 3. We note that when $L_{base} = L_{p^-}$, the base resistance of the polysilicon emitter power transistor with the buried P^+ grid reduces by a significant factor when compared to a similar structure with no buried P^+ grid. However, it should be noted that since here only 50% of the base region is effective, the current gain of this transistor will be smaller than that of the conventional transistor with no buried P^+ grid. We also note that even if L_{base} is 10 times L_{p^+}, i.e. if we introduce only 18 buried P^+ grid stripes under the emitter of Fig. 1, the base resistance can still be reduced by almost an order of magnitude while keeping the effective base area close to 90% and hence keeping the current gain of the transistor nearly unaffected. Therefore, it is clear that the buried P^+ grid is very effective in keeping the base resistance at a very small value thus reducing the adverse effects of emitter current crowding on the power transistor high current performance.

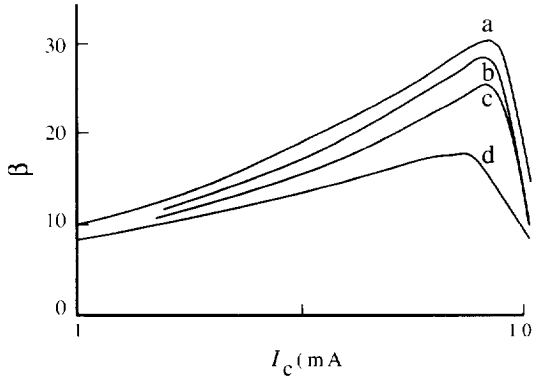

Fig. 4. Measured d.c. current gain vs collector current for (a) a conventional base with no buried P^+ grid under the emitter. (b) with $L_{p^-} = 5\,\mu$m, $L_{base} = 15\,\mu$m, (c) with $L_{p^-} = 5\,\mu$m, $L_{base} = 10\,\mu$m, and (d) with $L_{p^-} = 5\,\mu$m, $L_{base} = 5\,\mu$m.

EFFECT OF BURIED P^+ GRID ON CURRENT GAIN

The introduction of the buried P^+ grid affects the current gain due to the increased hole injection from the P^+ grid into the emitter. The buried P^+ grid also increases the effective base-Gummel number. The measured values of d.c. current gain β as a function of collector current are shown in Fig. 4 for the four test devices. The conventional base polyemitter transistor with no buried P^+ grid under the emitter has a peak current gain of 30. However, with the introduction of P^+ buried layer and with increasing L_{base}/L_{p+} ratio, the current gain decreases as predicted. We note from Fig. 3 that when $L_{base}/L_{p+} = 3$, there is a significant reduction in base resistance (by a factor of 20) while from Fig. 4, it is clear that for $L_{base}/L_{p+} = 3$, the decrease in d.c. current gain is negligible (it falls from 31 to about 28). Therefore, it seems reasonable to use a buried P^+ grid with $3L_{p+} = L_{base}$ to obtain the effect of interdigitation while keeping the current gain unaffected.

CONCLUSIONS

In this work, we have demonstrated the application of a novel buried P^+ grid to the polysilicon emitter power transistors to replace the traditional interdigitated emitter. We have shown that the base resistance of the transistor can be reduced significantly with the use of a buried P^+ grid without any deleterious effect on the current gain. Our novel structure results in efficient silicon surface utilization since it does not need the commonly used interdigitated emitter pattern. The fabrication of these devices is simple and compatible with conventional power transistor fabrication and should result in reduced emitter current crowding.

Acknowledgements—This work was supported by the NSERC and ITRC under research grants.

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